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1 Ordering Information

[Table 1] 8Gb DDR4 Ordering Information table

Part No.	Density	Organization	Bank	Voltage	PKG	Speed/Temp
CS66DU8GQ9	8G	x16	8	1.2V	96 Ball (7.5x13.3)	1600Mhz /-40~95°C

2 Key Features

[Table 2] 8Gb DDR4 Speed Bins

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	22-22-22	
tCK	1.25	1.071	0.937	0.833	0.75	0.682	0.625	ns
CAS Latency	11	13	15	17	19	21	22	nCK
tRCD	13.75	13.92	14.06	14.16	14.25	14.32	13.75	ns
tRP	13.75	13.92	14.06	14.16	14.25	14.32	13.75	ns
tRAS	35	34	33	32	32	32	32	ns
tRC	48.75	47.92	47.06	46.16	46.25	46.32	45.75	ns

- JEDEC standard 1.2V (1.14V~1.26V)
- $V_{DDQ} = 1.2V(1.14V\sim 1.26V)$
- $V_{PP} = 2.5V(1.14V\sim 1.26V)$
- 800 MHz fCK for 1600Mb/sec/pin, 933 MHz fCK for 1866Mb/sec/pin, 1067MHz fCK for 2133Mb/sec/pin, 1200MHz fCK for 2400Mb/sec/pin, 1333MHz fCK for 2666Mb/sec/pin, 1467MHz fCK for 2933Mb/sec/pin, 1600MHz fCK for 3200Mb/sec/pin,
- 8 Banks (2 Bank Groups)
- Programmable CAS Latency (posted CAS): 10,11,12,13,14,15,16,17,18,19,20, 21, 22, 23, 24
- Programmable CAS Write Latency (CWL) = 9,11 (DDR4-1600), 10,12 (DDR4-1866),11,14 (DDR4-2133),12,16 (DDR4-2400) and 14,18 (DDR4-2666) and 16, 20 (DDR4-3200)
- 8-bit pre-fetch
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal (self) calibration: Internal self calibration through ZQ pin (RZQ: 240 ohm \pm 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than $T_{CASE} 85^{\circ}C$, 3.9us at $85^{\circ}C < T_{CASE} < 95^{\circ}C$
- Connectivity Test Mode (TEN) is Supported
- Asynchronous Reset
- Package: 96 balls FBGA – x16
- All of Lead-Free products are compliant for RoHS
- All of products are Halogen-free
- CRC (Cyclic Redundancy Check) for Read/Write data security
- Command address parity check
- DBI (Data Bus Inversion)
- Gear down mode
- POD (Pseudo Open Drain) interface for data input/output
- Internal VREF for data inputs
- External VPP for DRAM Activating Power
- PPR and sPPR is supported

• The 8Gb DDR4 SDRAM is organized as a 64Mbit x16 I/Os x 8banks device.
 This synchronous device achieves high speed double-data-rate transfer rates of up to 3200Mb/sec/pin (DDR4-3200) for general applications.
 The chip is designed to comply with the following key DDR4 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset.
 All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and $_CK$ falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and $_DQS$) in a source synchronous fashion.
 The address bus is used to convey row, column, and bank address information in a $_RAS/_CAS$ multiplexing style. The DDR4 device operates with a single 1.2V (1.14V~1.26V) power supply. 1.2V (1.14V~1.26V) V_{DDQ} and 2.5V (2.375V~2.75V) V_{PP} .
 The 8Gb DDR4 device is available in 96ball FBGAs(x16).

- NOTE :
- 1) This data sheet is an abstract of full DDR4 specification and does not cover the common features which are described in "DDR4 SDRAM Device Operation & Timing Diagram".
 - 2) The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation

3 Package pinout & Package Outline

3.1 Package Pinout (TOP view) :

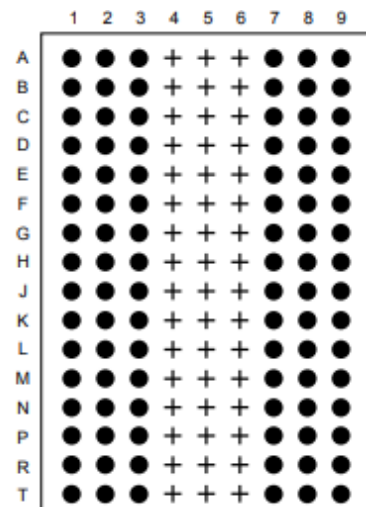
96ball TFBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n	VDD	L
M	VREFCA	BG0	A10/AP				A12/BC_n	CAS_n/ A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T

Ball Locations (x16)

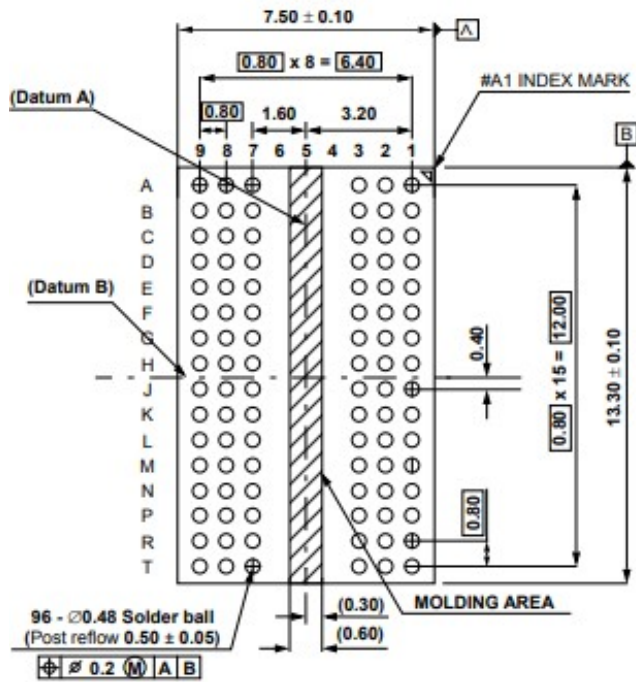
- Populated ball
- + Ball not populated

Top view
(See the balls through the package)

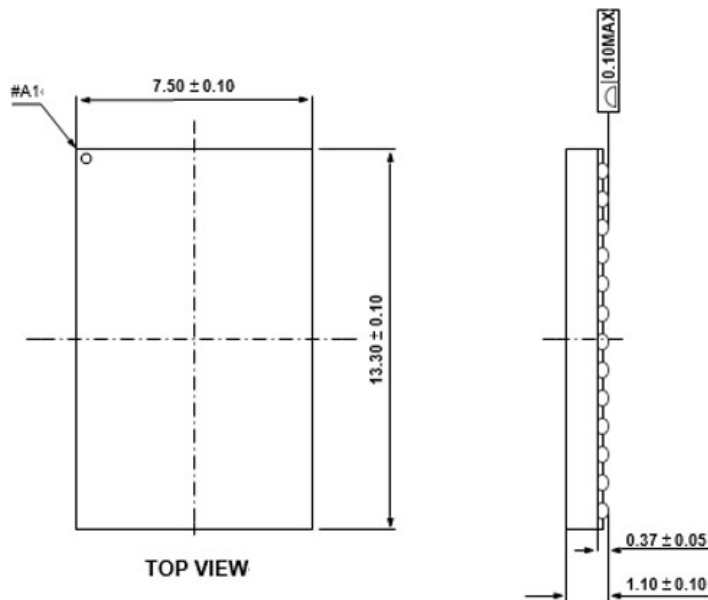


3.2 Package Outline

Units : Millimeters



BOTTOM VIEW



TOP VIEW

4. Input/Output Functional Description

[Table 3] Input/Output Function Description

Symbol	Type	Description
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configurations ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	I/O	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD
DQ	I/O	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	I/O	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.

[Table 3] Input/Output Function Description

Symbol	Type	Description
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/ TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/ TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0, and C0-C2 (3DS devices). Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is low.
ALERT_n	I/O	Alert : It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

NOTE :

1) Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination

5. DDR4 SDRAM ADDRESSING

2Gb Addressing Table

Configuration		128Mb x16
Bank Address	# of Bank Groups	2
	BG Address	BG0
	Bank Address in a BG	BA0~BA1
Row Address		A0~A13
Column Address		A0~A9
Page size		2KB

4Gb Addressing Table

Configuration		256Mb x16
Bank Address	# of Bank Groups	2
	BG Address	BG0
	Bank Address in a BG	BA0~BA1
Row Address		A0~A14
Column Address		A0~A9
Page size		2KB

8Gb Addressing Table

Configuration		512Gb x16
Bank Address	# of Bank Groups	2
	BG Address	BG0
	Bank Address in a BG	BA0~BA1
Row Address		A0~A15
Column Address		A0~A9
Page size		2KB

NOTE :

1) Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered.

Page size is per bank, calculated as follows:

$$\text{page size} = 2^{\text{COLBITS}} * \text{ORG} \div 8$$

where, COLBITS = the number of column address bits,

ORG = the number of I/O (DQ) bits

6. Absolute Maximum Ratings

[Table 4] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V _{IN} , V _{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5
T _{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :

- 1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
- 2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- 3) VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV
- 4) VPP must be equal or greater than VDD/VDDQ at all times.
- 5) Overshoot area above 1.5 V is specified in 8.3.4 Address, Command and Control Overshoot and Undershoot specifications, 8.3.5 Clock Overshoot and Undershoot Specifications and 8.3.6 Data, Strobe and Mask Overshoot and Undershoot Specifications.

6.1 DRAM Component Operating Temperature Range

[Table 5] Temperature Range

Symbol	Parameter	Rating	Unit	NOTE
T _{OPER}	Operating Temperature Range - Commercial	0 to 95	°C	1, 2, 3
	Operating Temperature Range - Industrial	-40 to 95	°C	1, 2, 3

NOTE :

- 1) Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM.
- 2) The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.
- 3) Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
- 4) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.
- 5) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

7. AC & DC Operating Conditions

[Table 6] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

NOTE :

- 6) Under all conditions V_{DDQ} must be less than or equal to V_{DD} .
- 7) V_{DDQ} tracks with V_{DD} . AC parameters are measured with V_{DD} and V_{DDQ} tied together.
- 8) DC bandwidth is limited to 20MHz.

[Table 7] Recommended Operating Temperature Ranges

Parameter/Condition	Min	Max-Normal	Max-Extended
Industrial Temperature	-40°C	85°C	95°C

NOTE :

- 1) The operating temperature is the case surface temperature on the center-top side of the DDR4 device. For measurements conditions, refer to JESD51-2.

8. AC & DC Input Measurement Levels

8.1 AC And DC Logic Input Levels for Single-Ended Signals

[Table 8] Single-ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933/3200		Unit	NOTE
		Min.	Max.	Min.	Max.		
$V_{IH,CA}(DC75)$	DC input logic high	$V_{REFCA} + 0.075$	VDD	-	-	V	
$V_{IL,CA}(DC75)$	DC input logic low	VSS	$V_{REFCA} - 0.075$	-	-	V	
$V_{IH,CA}(DC65)$	DC input logic high	-	-	$V_{REFCA} + 0.065$	VDD	V	
$V_{IL,CA}(DC65)$	DC input logic low	-	-	VSS	$V_{REFCA} - 0.065$	V	
$V_{IH,CA}(AC100)$	AC input logic high	$V_{REF} + 0.1$	Note 2	-	-	V	1
$V_{IL,CA}(AC100)$	AC input logic low	Note 2	$V_{REF} - 0.1$	-	-	V	1
$V_{IH,CA}(AC90)$	AC input logic high	-	-	$V_{REF} + 0.09$	Note 2	V	1
$V_{IL,CA}(AC90)$	AC input logic low	-	-	Note 2	$V_{REF} - 0.09$	V	1
$V_{REFCA}(DC)$	Reference Voltage for ADD, CMD inputs	$0.49 \cdot VDD$	$0.51 \cdot VDD$	$0.49 \cdot VDD$	$0.51 \cdot VDD$	V	2,3

- NOTE :**
- 1) See "Overshoot and Undershoot Specifications" on section 8.3 AC and DC Logic Input Levels for Differential Signals.
 - 2) The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than $\pm 1\%$ VDD (for reference : approx. $\pm 12mV$)
 - 3) For reference : approx. $VDD/2 \pm 12mV$

8.2 AC and DC Input Measurement Levels: VREF Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 1. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA}).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 10. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than $\pm 1\%$ V_{DD} .

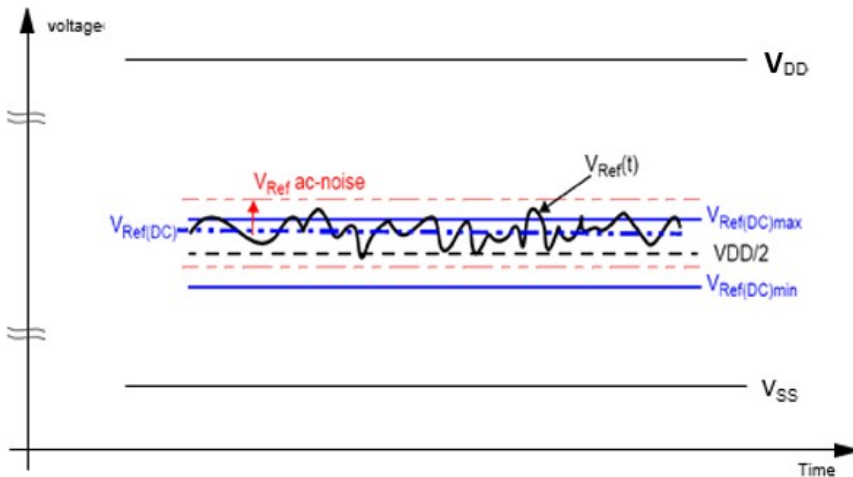


Figure 1. Illustration of $V_{REF}(DC)$ tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF} .

" V_{REF} " shall be understood as $V_{REF}(DC)$, as defined in Figure 1.

This clarifies that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit ($\pm 1\%$ of V_{DD}) are included in DRAM timings and their associated deratings.

8.3 AC and DC Logic Input Levels for Differential Signals

8.31 Differential Signals Definition

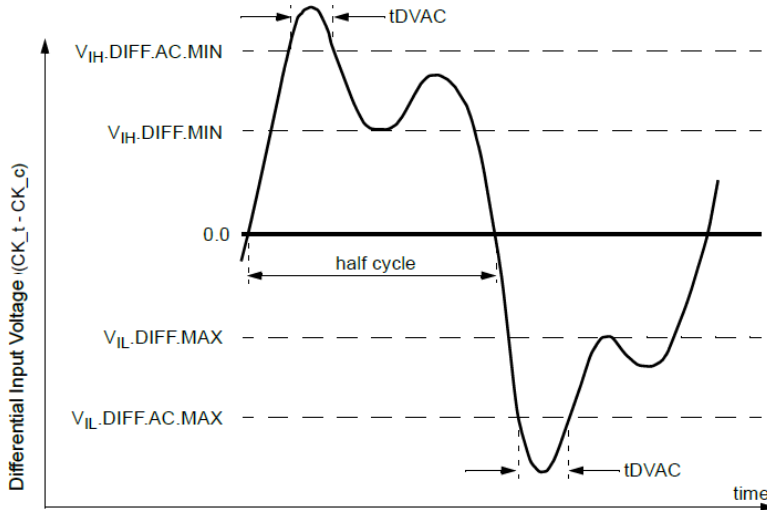


Figure 2. Definition of differential ac-swing and “time above ac-level” tDVAC

NOTE :

- 1) Differential signal rising edge from V_{IL,DIFF.MAX} to V_{IH,DIFF.MIN} must be monotonic slope.
- 2) Differential signal falling edge from V_{IH,DIFF.MIN} to V_{IL,DIFF.MAX} must be monotonic slope

8.32 Differential Swing Requirements for Clock (CK_t - CK_c)

[Table 9] Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		DDR4 -2400/2666		DDR4-2933		DDR4-3200		unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
V _{IHdiff}	differential input high	150	NOTE 3	135	NOTE 3	125	NOTE 3	110	NOTE 3	mV	1
V _{ILdiff}	differential input low	NOTE 3	-150	NOTE 3	-135	NOTE 3	-125	NOTE 3	-110	mV	1
V _{IHdiff(AC)}	differential input high ac	2 x (V _{IH(AC)} - V _{REF})	NOTE 3	2 x (V _{IH(AC)} - V _{REF})	NOTE 3	2 x (V _{IH(AC)} - V _{REF})	NOTE 3	2 x (V _{IH(AC)} - V _{REF})	NOTE 3	mV	2
V _{ILdiff(AC)}	differential input low ac	NOTE 3	2 x (V _{IL(AC)} - V _{REF})	NOTE 3	2 x (V _{IL(AC)} - V _{REF})	NOTE 3	2 x (V _{IL(AC)} - V _{REF})	NOTE 3	2 x (V _{IL(AC)} - V _{REF})	mV	

NOTE :

- 1) Used to define a differential signal slew-rate.
- 2) for CK_t - CK_c use V_{IH,CA}/V_{IL,CA(AC)} of ADD/CMD and V_{REFCA};
- 3) These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits (V_{IH,CA(DC)} max, V_{IL,CA(DC)} min) for single-ended signals as well as the limitations for overshoot and undershoot.

[Table 10] Allowed Time Before Ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	tDVAC [ps] @ V _{IH/Ldiff(AC)} = 200mV	
	min	max
> 4.0	120	-
4.0	115	-
3.0	110	-
2.0	105	-
1.8	100	-
1.6	95	-
1.4	90	-
1.2	85	-
1.0	80	-
< 1.0	80	-

8.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach V_{SEH}min / V_{SEL}max (approximately equal to the ac-levels (V_{IH}.CA(AC) / V_{IL}.CA(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than V_{IH}.CA(AC100)/V_{IL}.CA(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c.

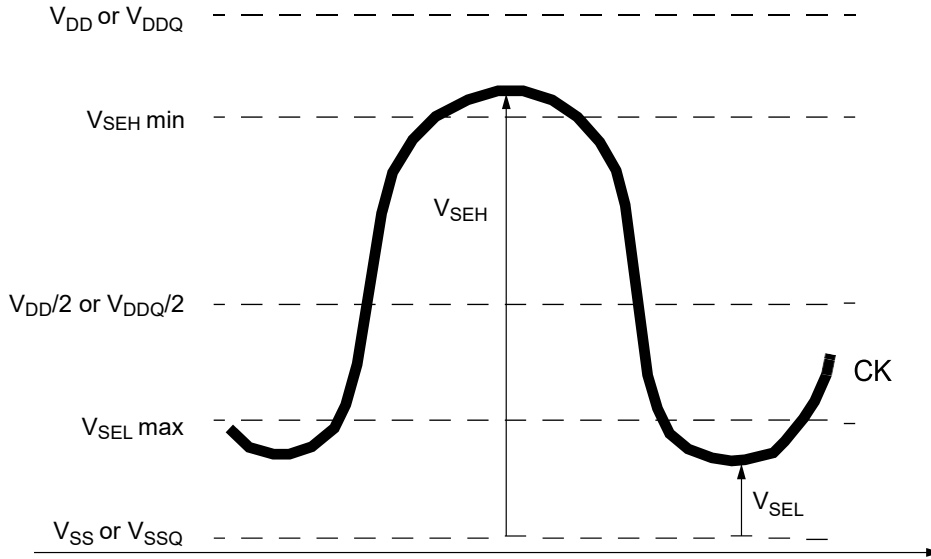


Figure 3. Single-ended requirement for differential signals

Note that, while ADD/CMD signal requirements are with respect to V_{refCA}, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single ended components of differential signals the requirement to reach V_{SEL}max, V_{SEH}min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 11] Single-ended Levels for CK_t, CK_c

Sym- bol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933		DDR4-3200		Un it	NOT E
		Min	Max	Min	Max	Min	Max	Min	Max		
V _{SEH}	Single-ended high-level for CK _t , CK _c	(VDD/2)+0.100	NOTE3	(VDD/2)+0.095	NOTE3	(VDD/2)+0.085	NOTE3	(VDD/2)+0.085	NOTE3	V	1, 2
V _{SEL}	Single-ended low-level for CK _t , CK _c	NOTE3	(VDD/2)-0.100	NOTE3	(VDD/2)-0.095	NOTE3	(VDD/2)-0.085	NOTE3	(VDD/2)-0.085	V	1, 2

NOTE :

- 1) For CK_t - CK_c use V_{IH}.CA/V_{IL}.CA(AC) of ADD/CMD;
- 2) V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};
- 3) These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits (V_{IH}.CA(DC) max, V_{IL}.CA(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

8.3.4 Address, Command and Control Overshoot and Undershoot specifications

[Table 12] AC overshoot/undershoot specification for Address, Command and Control pins

Parameter	Symbol	Specification							Unit	NOT E
		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
Maximum peak amplitude above VAOS	V_{AOSP}	0.06							V	
Upper boundary of overshoot area AAOS1	V_{AOS}	VDD +0.24							V	1
Maximum peak amplitude allowed for undershoot	V_{AUS}	0.30							V	
Maximum overshoot area per 1 tCK above VAOS	A_{AOS2}	0.0083	0.0071	0.0062	0.0055	0.0055	0.0055	0.0055	V-ns	
Maximum overshoot area per 1 tCK between VDD and VAOS	A_{AOS1}	0.2550	0.2185	0.1914	0.1699	0.1699	0.1699	0.1699	V-ns	
Maximum undershoot area per 1 tCK below VSS	A_{AUS}	0.2644	0.2265	0.1984	0.1762	0.1762	0.1762	0.1762	V-ns	
(A0-A13,A17,BG0-BG1,BA0-BA1,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0)										

NOTE :

- 1) The value of VAOS matches VDD absolute max as defined in Table 6 Absolute Maximum DC Ratings if VDD equals VDD max as defined in Table 8 Recommended DC Operating Conditions. If VDD is above the recommended operating conditions, VAOS remains at VDD absolute max as defined in Table 4.

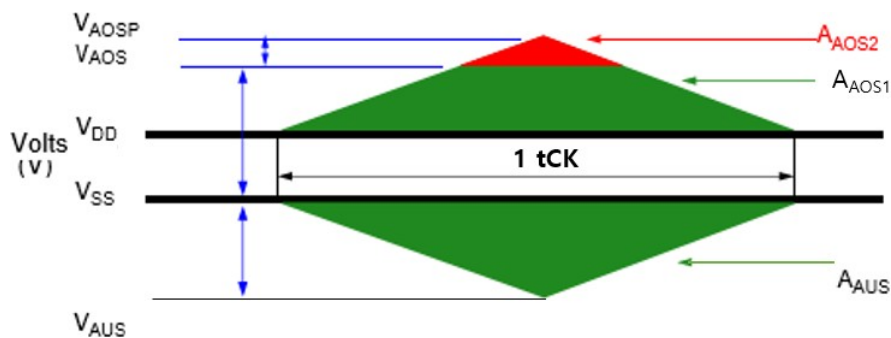


Figure 4. Address, Command and Control Overshoot and Undershoot Definition

8.3.5 Clock Overshoot and Undershoot Specifications

[Table 13] AC overshoot/undershoot specification for Clock

Parameter	Symbol	Specification							Unit	Note
		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
Maximum peak amplitude above VCOS	V_{COSP}	0.06							V	
Upper boundary of overshoot area ADOS1	V_{COS}	VDD +0.24							V	1
Maximum peak amplitude allowed for undershoot	V_{CUS}	0.30							V	
Maximum overshoot area per 1 UI above VCOS	A_{COS2}	0.0038	0.0032	0.0028	0.0025	0.0025	0.0025	0.0025	V-ns	
Maximum overshoot area per 1 UI between VDD and VDOS	A_{COS1}	0.1125	0.0964	0.0844	0.0750	0.0750	0.0750	0.0750	V-ns	
Maximum undershoot area per 1 UI below VSS	A_{CUS}	0.1144	0.0980	0.0858	0.0762	0.0762	0.0762	0.0762	V-ns	
(CK_t, CK_c)										

NOTE :

- The value of VCOS matches VDD absolute max as defined in Table 6 Absolute Maximum DC Ratings if VDD equals VDD max as defined in Table 8 Recommended DC Operating Conditions. If VDD is above the recommended operating conditions, VCOS remains at VDD absolute max as defined in Table 4.

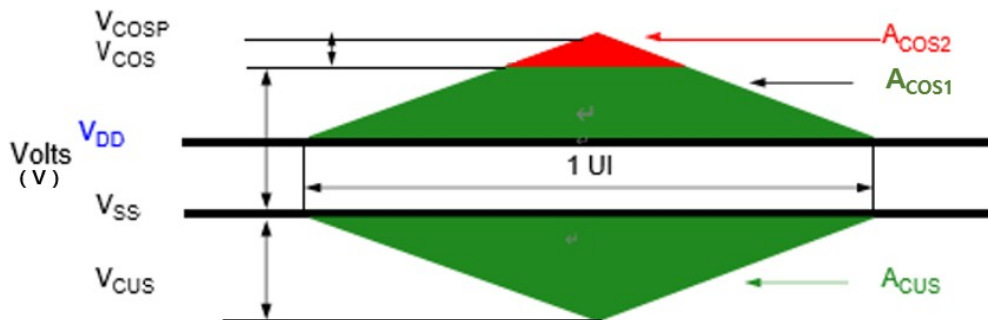


Figure 5. Clock Overshoot and Undershoot Definition

8.3.6 Data, Strobe and Mask Overshoot and Undershoot Specifications

[Table 14] AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Symbol	Specification							Unit	Note
		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200		
Maximum peak amplitude above VDOS	V_{DOSP}	0.16							V	
Upper boundary of overshoot area ADOS1	V_{DOS}	$V_{DDQ} + 0.24$							V	1
Lower boundary of undershoot area ADUS1	V_{DUS}	0.30							V	2
Maximum peak amplitude below VDUS	V_{DUSP}	0.10							V	
Maximum overshoot area per 1 UI above VDOS	A_{DOS2}	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V-ns	
Maximum overshoot area per 1 UI between VDDQ and VDOS	A_{DOS1}	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V-ns	
Maximum undershoot area per 1 UI between VSSQ and VDUS1	A_{DUS1}	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V-ns	
Maximum undershoot area per 1 UI below VDUS	A_{DUS2}	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V-ns	

NOTE :
 1) The value of VDOS matches (VIN, VOUT) max as defined in Table 6 Absolute Maximum DC Ratings if VDDQ equals VDDQ max as defined in Table 6 Recommended DC Operating Conditions. If VDDQ is above the recommended operating conditions, VDOS remains at (VIN, VOUT) max as defined in Table 4.
 2) The value of VDUS matches (VIN, VOUT) min as defined in Table 4 Absolute Maximum DC Ratings

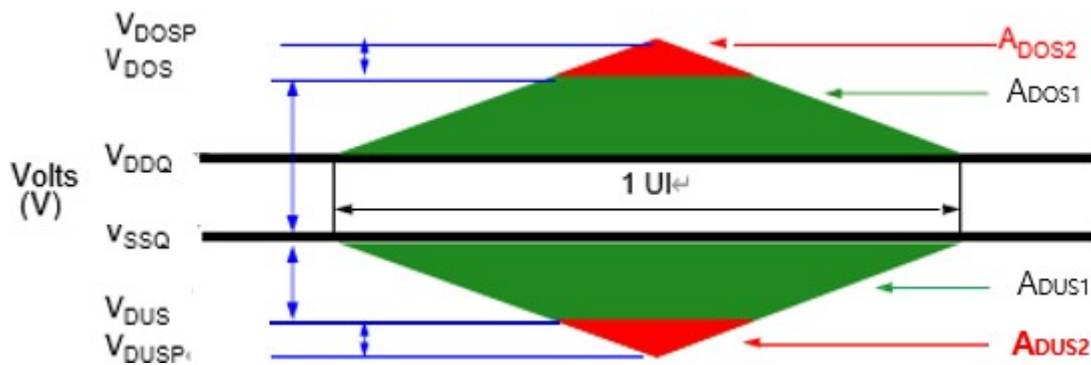


Figure 6. Data, Strobe and Mask Overshoot and Undershoot Definition

8.4 Slew Rate Definitions

8.4.1 Slew Rate Definitions for Differential Input Signals (CK)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table 15 and Figure 7.

[Table 15] Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK _t - CK _c)	V _{ILdiffmax}	V _{IHdiffmin}	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TR_{diff}$
Differential input slew rate for falling edge (CK _t - CK _c)	V _{IHdiffmin}	V _{ILdiffmax}	$[V_{IHdiffmin} - V_{ILdiffmax}] / \Delta TF_{diff}$

NOTE :

- 1) The differential signal (i.e.,CK_t - CK_c) must be linear between these thresholds.

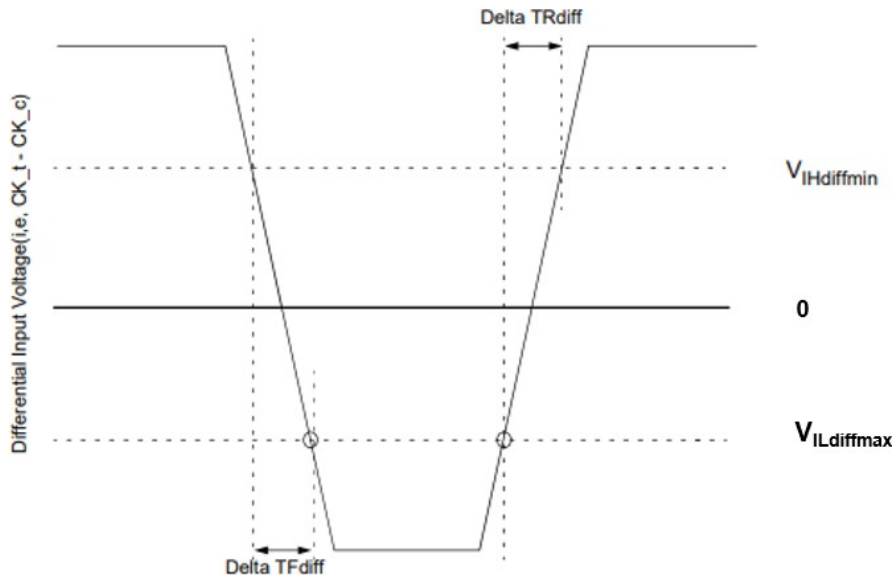


Figure 7. Differential Input Slew Rate Definition for CK_t, CK_c

8.4.2 Slew Rate Definition for Single-ended Input Signals (CMD/ADD)

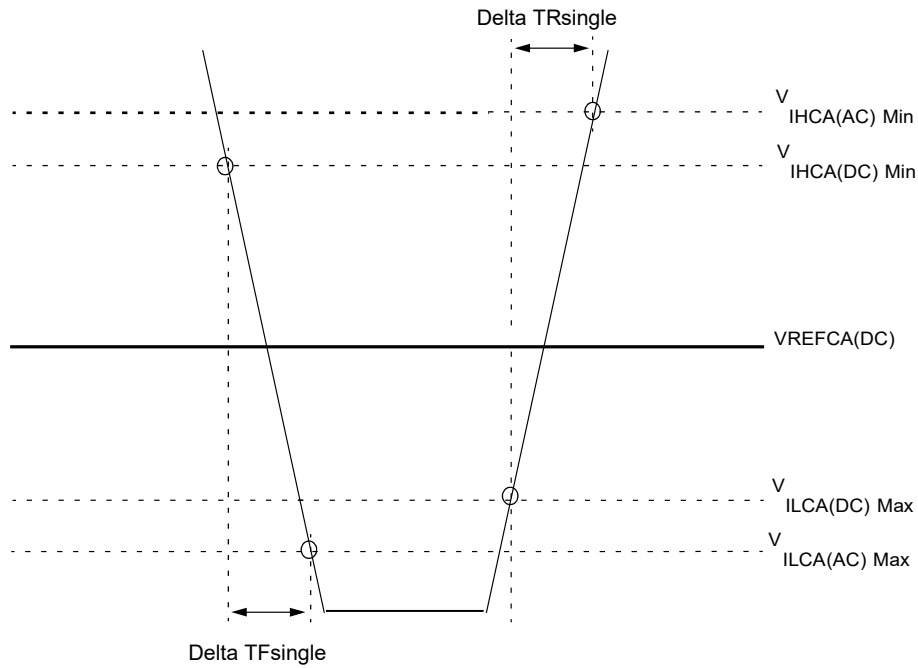


Figure 8. Single-ended Input Slew Rate Definition for CMD and ADD

NOTE :

- 1) Single-ended input slew rate for rising edge = $\{V_{IHCA(AC)Min} - V_{ILCA(DC)Max}\} / \Delta T_{Rsingle}$.
- 2) Single-ended input slew rate for falling edge = $\{V_{IHCA(DC)Min} - V_{ILCA(AC)Max}\} / \Delta T_{Fsingle}$.
- 3) Single-ended signal rising edge from $V_{ILCA(DC)Max}$ to $V_{IHCA(DC)Min}$ must be monotonic slope.
- 4) Single-ended signal falling edge from $V_{IHCA(DC)Min}$ to $V_{ILCA(DC)Max}$ must be monotonic slope.

8.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 16. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

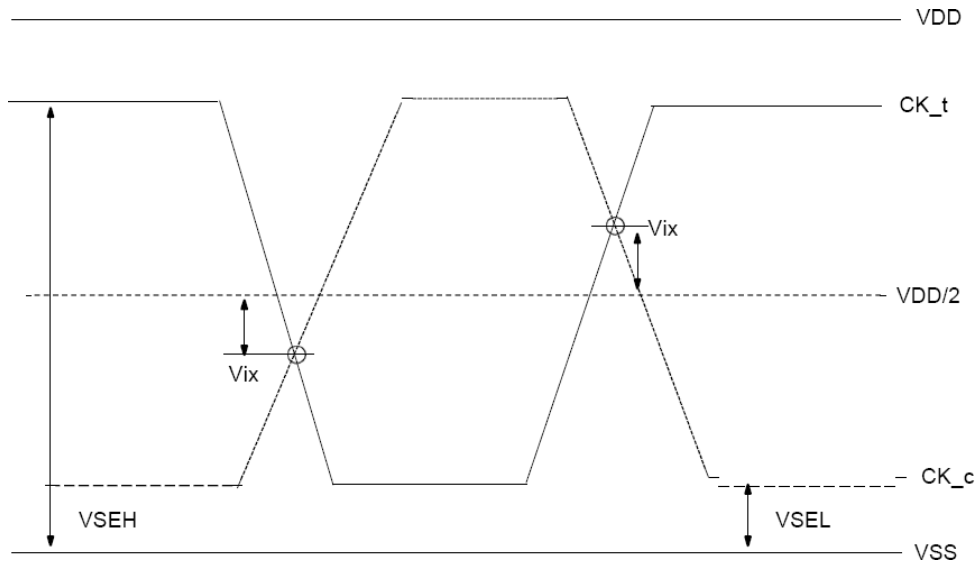


Figure 9. Vix Definition (CK)

[Table 16] Cross Point Voltage for Differential Input Signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133/2400			
		min		max	
-	Area of VSEH, VSEL	$VSEL < VDD/2 - 145mV$	$VDD/2 - 145mV \leq VSEL \leq VDD/2 - 100mV$	$VDD/2 + 100mV \leq VSEH \leq VDD/2 + 145mV$	$VDD/2 + 145mV < VSEH$
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK _t , CK _c	-120 mV	$-(VDD/2 - VSEL) + 25mV$	$(VSEH - VDD/2) - 25mV$	120mV

Symbol	Parameter	DDR4-2666/2933/3200			
		min		max	
-	Area of VSEH, VSEL	$VSEL < VDD/2 - 145 mV$	$VDD/2 - 145 mV \leq VSEL \leq VDD/2 - 100 mV$	$VDD/2 + 100 mV \leq VSEH \leq VDD/2 + 145 mV$	$VDD/2 + 145 mV < VSEH$
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK _t , CK _c	-110 mV	$-(VDD/2 - VSEL) + 30 mV$	$(VSEH - VDD/2) - 30 mV$	110mV

8.6 CMOS rail to rail Input Levels

8.6.1 CMOS rail to rail Input Levels for RESET_n

[Table 17] CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rising time	TR_RESET	-	1.0	us	4
RESET pulse width	tPW_RESET	1.0	-	us	3,5

NOTE :

- 1) After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not bereset.
- 2) Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
- 3) RESET is destructive to data contents.
- 4) No slope reversal (ringback) requirement during its level transition from Low to High.
- 5) This definition is applied only "Reset Procedure at Power Stable".
- 6) Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
- 7) Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

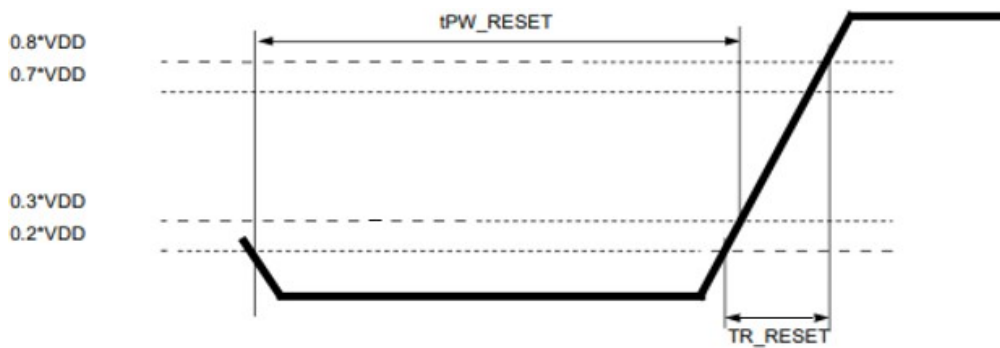


Figure 10. RESET_n Input Slew Rate Definition

8.7 AC and DC Logic Input Levels for DQS Signals

8.7.1 Differential signal definition

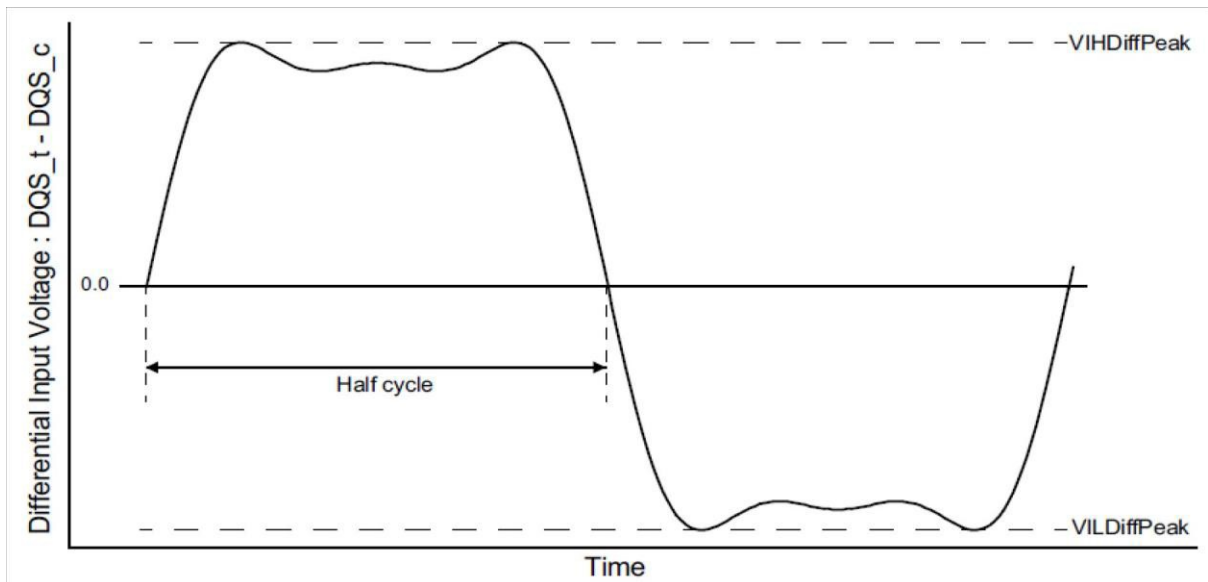


Figure 11. Definition of differential DQS Signal AC-swing Level

8.7.2 Differential swing requirements for DQS (DQS_t - DQS_c)

[Table 18] Differential AC and DC Input Levels for DQS

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	186	Note2	160	Note2	150	Note2	145	Note2	140	Note2	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note2	-186	Note2	-160	Note2	-150	Note2	-145	Note2	-140	mV	1

NOTE :

- 1) Used to define a differential signal slew-rate.
- 2) These values are not defined; however, the differential signals DQS_t - DQS_c, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

8.7.3 Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.

$$VIH.DIFF.Peak Voltage = \text{Max}(f(t))$$

$$VIL.DIFF.Peak Voltage = \text{Min}(f(t))$$

$$f(t) = VDQS_t - VDQS_c$$

The $\text{Max}(f(t))$ or $\text{Min}(f(t))$ used to determine the midpoint which to reference the +/-35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all UIs.

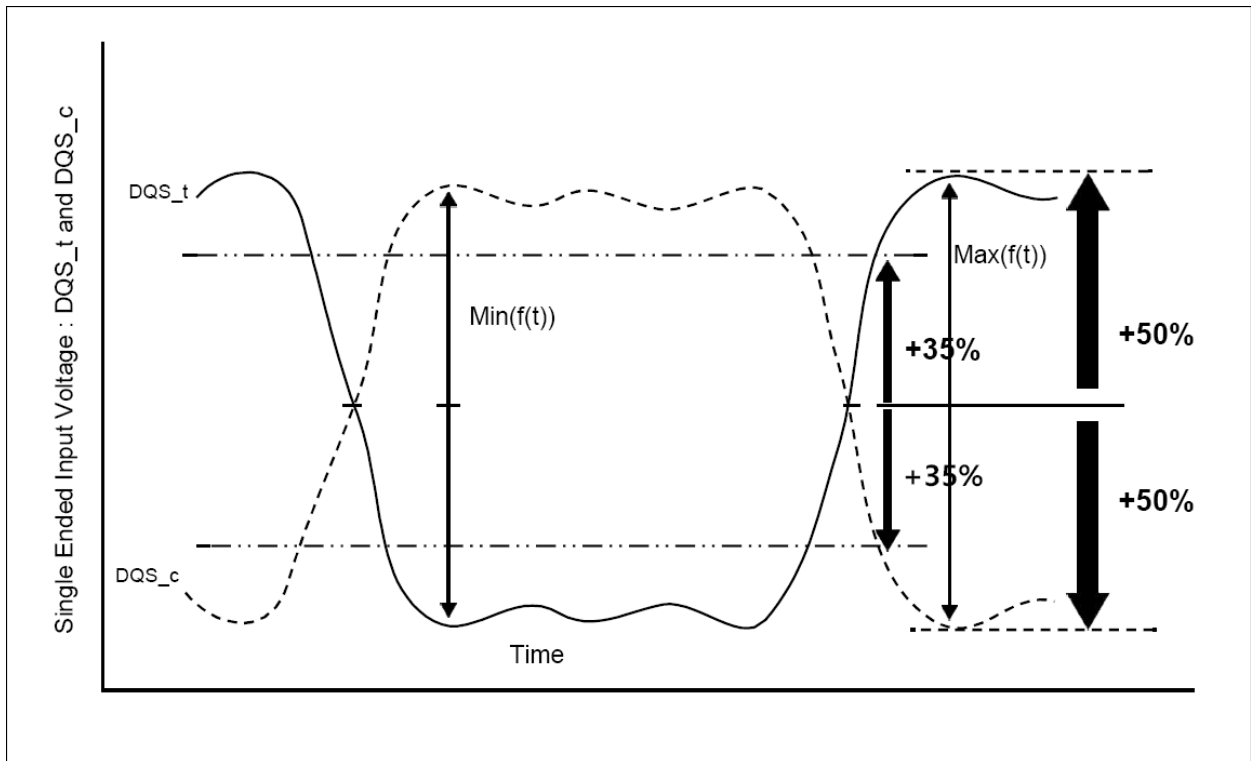


Figure 12. Definition of differential DQS Peak Voltage and range of exempt non-monotonic signaling

8.7.4 Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 21. The differential input cross point voltage VIX_DQS (VIX_DQS_FR and VIX_DQS_RF) is measured from the actual cross point of DQS_t, DQS_c relative to the VDQSmid of the DQS_t and DQS_c signals.

VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.

A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 35% of the midpoint of either VIH.DIFF.Peak Voltage (DQS_t rising) or VIL.DIFF.Peak Voltage (DQS_c rising), refer to Figure 12. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure 13) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure 13) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure 13) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure 13) is not a valid horizontal tangent

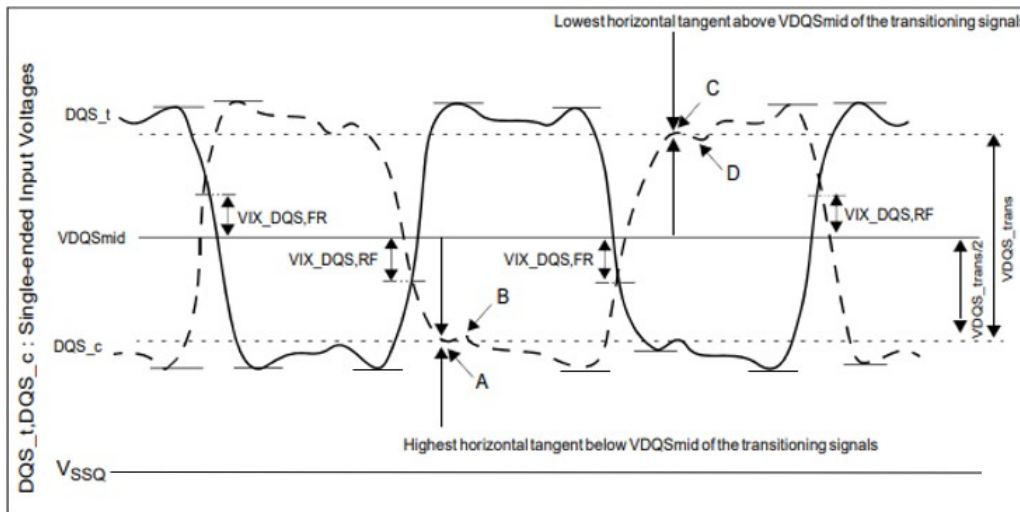


Figure 13. Vix Definition (DQS)

[Table 19] Cross point voltage for DQS differential input signals

Symbol	Parameter	DDR4-1600/1866/2133/ 2400		DDR4-2666/2933/3200		Unit	Note
		Min	Max	Min	Max		
Vix_DQS_ratio	DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	-	25	-	25	%	1, 2
VDQSmid_to_Vcent	VDQSmid offset relative to Vcent_DQ(midpoint)	-	min (VIHdiff,50)	-	min (VIHdiff,50)	mV	3, 4, 5

NOTE :

- 1) Vix_DQS_Ratio is DQS VIX crossing (Vix_DQS_FR or Vix_DQS_RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
- 2) VDQSmid will be similar to the VREFDQ internal setting value obtained during Vref Training if the DQS and DQs drivers and paths are matched.
- 3) The maximum limit shall not exceed the smaller of VIHdiff minimum limit or 50mV.
- 4) VIX measurements are only applicable for transitioning DQS_t and DQS_c signals when toggling data, preamble and high-z states are not applicable conditions.
- 5) The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

8.7.5 Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 13 and Figure 14.

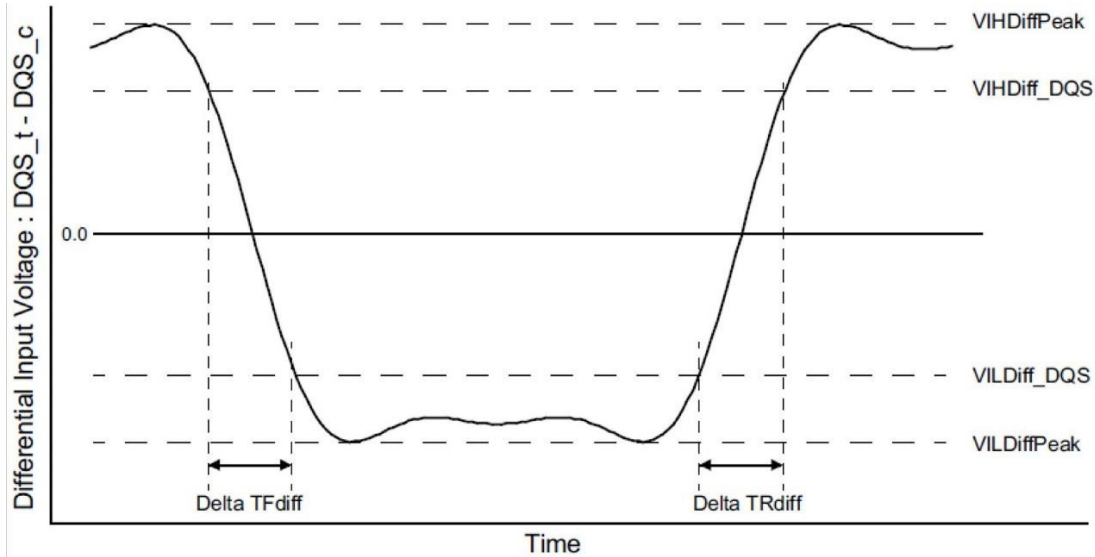


Figure 14. Differential Input Slew Rate Definition for DQS_t, DQS_c

NOTE :

- 1) Differential signal rising edge from VILDif_DQS to VIHDiff_DQS must be monotonic slope.
- 2) Differential signal falling edge from VIHDiff_DQS to VILDif_DQS must be monotonic slope.

[Table 20] Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (DQS_t - DQS_c)	VILDif_DQS	VIHDiff_DQS	$ VILDif_DQS - VIHDiff_DQS / \Delta TRdiff$
Differential input slew rate for falling edge (DQS_t - DQS_c)	VIHDiff_DQS	VILDif_DQS	$ VILDif_DQS - VIHDiff_DQS / \Delta TFdiff$

[Table 21] Differential Input Level for DQS_t, DQS_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933		DDR4-3200		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max		
VIHDiff_DQS	Differential Input High	136	-	130	-	115	-	110	-	mV	
VILDif_DQS	Differential Input Low	-	-136	-	-130	-	-115	-	-110	mV	

[Table 22] Differential Input Slew Rate for DQS_t, DQS_c

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933/3200		Unit	NOTE
		Min	Max	Min	Max		
SRIdiff	Differential Input Slew Rate	3	18	2.5	18	V/ns	

9. AC & DC OUTPUT MEASUREMENT LEVELS

9.1 Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors ($R_{ON_{pu}}$ and $R_{ON_{pd}}$) are defined as follows:

$$R_{ON_{pu}} = \frac{V_{DDQ} - V_{out}}{|I_{out}|}$$

under the condition that $R_{ON_{pd}}$ is off

$$R_{ON_{pd}} = \frac{V_{out}}{|I_{out}|}$$

under the condition that $R_{ON_{pu}}$ is off

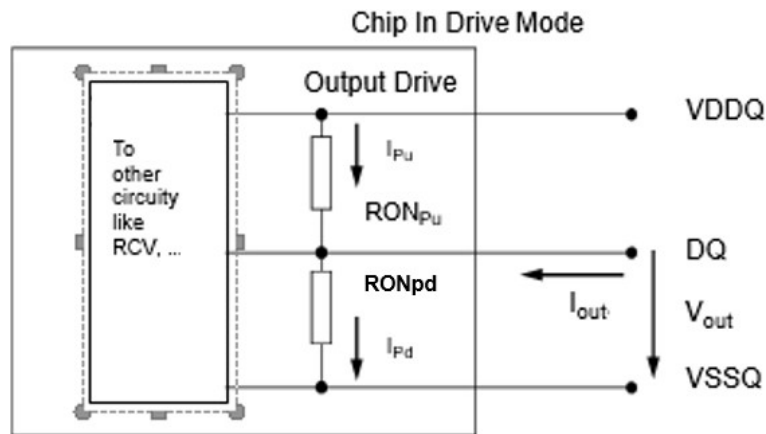


Figure 15. Output driver

[Table 23] Output Driver DC Electrical Characteristics, assuming RZQ=240ohm; entire operating temperature range; after proper ZQ calibration

RON _{NOM}	Resistor	V _{out}	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.65	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.75	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.75	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.65	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.75	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.75	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10	-	17	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4

NOTE:

- 1) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity. 9.1.1 Output Driver Temperature and Voltage Sensitivity.
- 2) Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 1.1 * VDDQ.
- 3) Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

- 4) RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

- 5) This parameter of x16 device is specified for Upper byte and Lower byte.

9.1.1 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the equations and tables below.

$$\Delta T = T - T(@\text{calibration}); \Delta V = VDDQ - VDDQ(@ \text{calibration}); VDD = VDDQ$$

[Table 24] Output Driver Sensitivity Definitions

Symbol	Min	Max	Unit
$R_{ONPU}@ V_{OH}(DC)$	$0.6 - dR_{ONdTH} \times \Delta T - dR_{ONdVH} \times \Delta V $	$1.1 - dR_{ONdTH} \times \Delta T + dR_{ONdVH} \times \Delta V $	$R_{ZQ}/6$
$R_{ON}@ V_{OM}(DC)$	$0.9 - dR_{ONdTM} \times \Delta T - dR_{ONdVM} \times \Delta V $	$1.1 + dR_{ONdTM} \times \Delta T + dR_{ONdVM} \times \Delta V $	$R_{ZQ}/6$
$R_{ONPD}@ V_{OL}(DC)$	$0.6 - dR_{ONdTL} \times \Delta T - dR_{ONdVL} \times \Delta V $	$1.1 + dR_{ONdTL} \times \Delta T + dR_{ONdVL} \times \Delta V $	$R_{ZQ}/6$

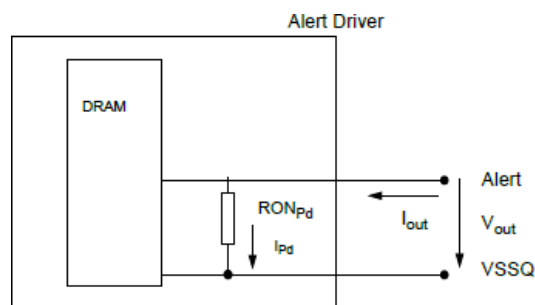
[Table 25] Output Driver Temperature and Voltage Sensitivity

Symbol	Voltage and Temperature Range		Unit
	Min	Max	
dR_{ONdTM}	0	1.5	%/°C
dR_{ONdVM}	0	0.15	%/mV
dR_{ONdTL}	0	1.5	%/°C
dR_{ONdVL}	0	0.15	%/mV
dR_{ONdTH}	0	1.5	%/°C
dR_{ONdVM}	0	0.15	%/mV

9.1.2 Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance R_{ON} is defined as follows:

$$R_{ON_{pd}} = \frac{V_{out}}{|I_{out}|} \quad \text{under the condition that } R_{ON_{pu}} \text{ is off}$$



Resistor	Vout	Min	Max	Unit	NOTE
R_{ONpd}	$V_{OLdc} = 0.1 * VDDQ$	0.3	1.2	34Ω	1
	$V_{OMdc} = 0.8 * VDDQ$	0.4	1.2	34Ω	1
	$V_{OHdc} = 1.1 * VDDQ$	0.4	1.4	34Ω	1

NOTE:
1) VDDQ voltage is at VDDQ DC.

9.1.3 Output Drive Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode.

The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows

$$RON_{Pu_CT} = \frac{V_{DDQ} - V_{out}}{|I_{out}|}$$

$$RON_{Pd_CT} = \frac{V_{out}}{|I_{out}|}$$

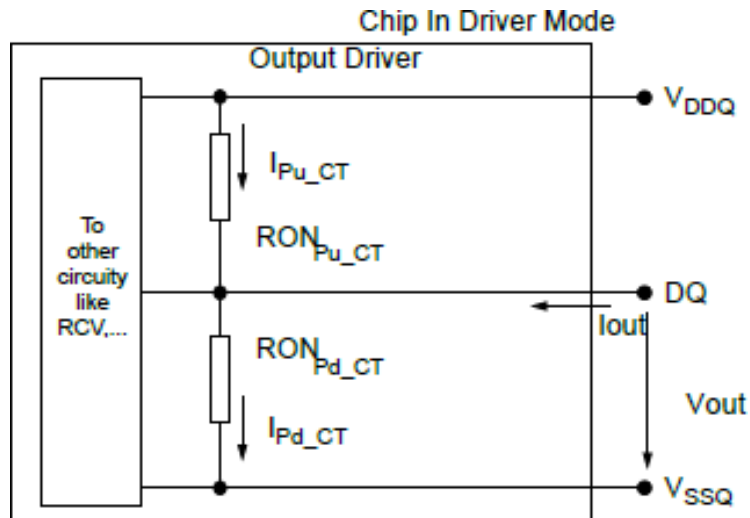


Figure 16. Output driver

RON _{NOM_CT}	Resistor	Vout	Max	Units	NOTE
34Ω	RON _{Pd_CT}	VOB _{dc} = 0.2 x V _{DDQ}	1.9	34Ω	1
		VOL _{dc} = 0.5 x V _{DDQ}	2.0	34Ω	1
		VOM _{dc} = 0.8 x V _{DDQ}	2.2	34Ω	1
	RON _{Pu_CT}	VOH _{dc} = 1.1 x V _{DDQ}	2.5	34Ω	1
		VOB _{dc} = 0.2 x V _{DDQ}	2.5	34Ω	1
		VOL _{dc} = 0.5 x V _{DDQ}	2.2	34Ω	1
		VOM _{dc} = 0.8 x V _{DDQ}	2.0	34Ω	1
		VOH _{dc} = 1.1 x V _{DDQ}	1.9	34Ω	1

NOTE :
2) Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

9.2 Single-ended AC & DC Output Levels

[Table 26] Single-ended AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200	Units	Note
V _{OH} (DC)	DC output high measurement level (for IV curve linearity)	1.1 x V _{DDQ}	V	
V _{OM} (DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V _{DDQ}	V	
V _{OL} (DC)	DC output low measurement level (for IV curve linearity)	0.5 x V _{DDQ}	V	
V _{OH} (AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x V _{DDQ}	V	1
V _{OL} (AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x V _{DDQ}	V	1

NOTE :

- 1) The swing of $\pm 0.15 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $RZQ/7\Omega$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

9.3 Differential AC&DC Output Levels

[Table 27] Differential AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200	Units	Note
V _{OHdiff} (AC)	AC differential output high measurement level (for output SR)	+0.3 x V _{DDQ}	V	1
V _{OLdiff} (AC)	AC differential output low measurement level (for output SR)	-0.3 x V _{DDQ}	V	1

NOTE :

- 1) The swing of $\pm 0.3 \times V_{DDQ}$ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of $RZQ/7\Omega$ and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each of the differential outputs.

9.4 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 28 and Figure 17.

[Table 28] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TR_{se}$
Single ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta TF_{se}$

NOTE :

1) Output slew rate is verified by design and characterization, and may not be subject to production test.

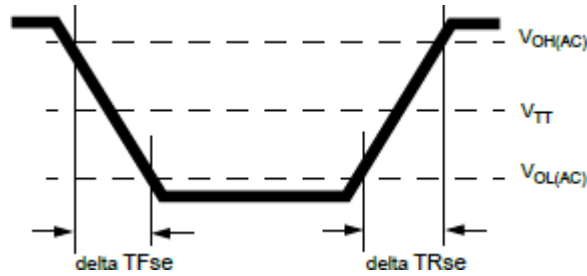


Figure 17. Single-ended Output Slew Rate Definition

[Table 29] Single-ended Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

NOTE :

1) In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.

- Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

- Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

9.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff}(AC)$ and $V_{OHdiff}(AC)$ for differential signals as shown in Table 30 and Figure 18.

[Table 30] Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / \Delta TR_{diff}$
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / \Delta TF_{diff}$

NOTE:

1) Output slew rate is verified by design and characterization, and may not be subject to production test.

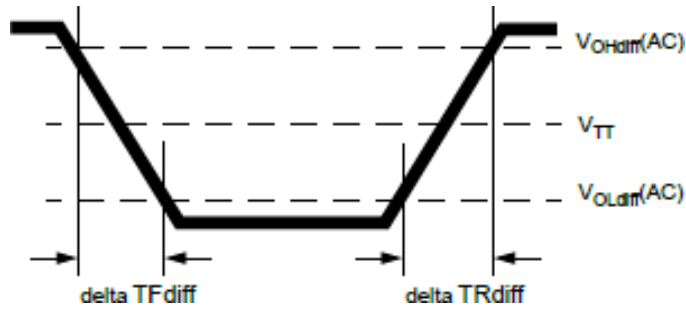


Figure 18. Differential Output Slew Rate Definition

[Table 31] Differential Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	8	18	8	18	8	18	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For Ron = RZQ/7 setting

9.6 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

[Table 32] Single-ended AC & DC Output Levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200		Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ		V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ		V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ		V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ		V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	$V_{TT} + (0.1 \times V_{DDQ})$		V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	$V_{TT} - (0.1 \times V_{DDQ})$		V	1

NOTE :

1) The effective test load is 50Ω terminated by $V_{TT} = 0.5 \times V_{DDQ}$.

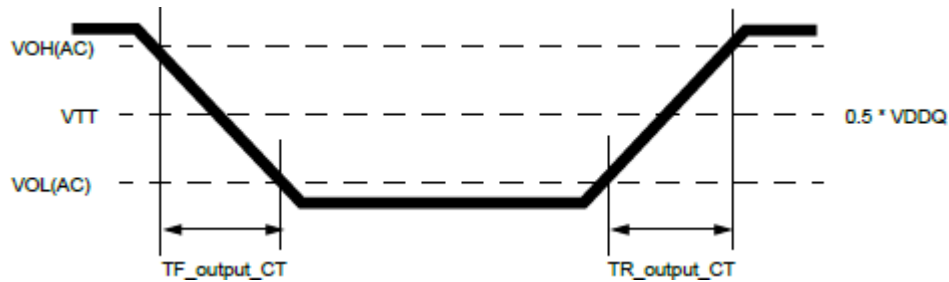


Figure 19. Output Slew Rate Definition of Connectivity Test Mode

[Table 33] Single-ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400/2666/2933/3200		Unit	Notes
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

9.7 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 20.

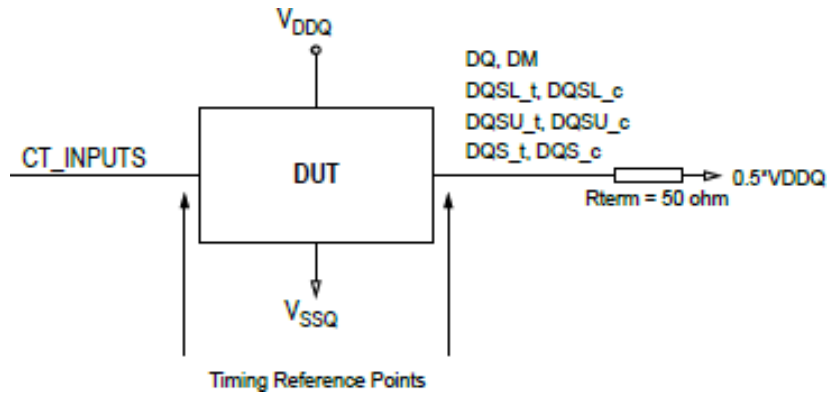


Figure 20. Connectivity Test Mode Timing Reference Load

10. Speed Bin

[Table 34] DDR4-1600 Speed Bins and Operations

Speed Bin			DDR4-1600		Unit	Note	
CL-nRCD-nRP			11-11-11				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		13.75 ¹⁴⁾ (13.50) ^{5),12)}	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 2nCK	tAA(max) + 2nCK	ns	12	
ACT to internal read or write delay time	tRCD		13.75 ¹⁴⁾ (13.50) ^{5),12)}	-	ns	12	
PRE command period	tRP		13.75 ¹⁴⁾ (13.50) ^{5),12)}	-	ns	12	
ACT to PRE command period	tRAS		35	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		48.75 ¹⁴⁾ (48.50) ^{5),12)}	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional) ^{5),12)}	tCK(AVG)	1.5 (Optional) ^{5),12),14)}	1.6	ns	1,2,3,4,11,17
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,17
CW CWL = 9, 11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings			(9),11,12		nCK	13,14	
Supported CL Settings with read DBI			(11),13,14		nCK	13	
Supported CWL Settings			9,11		nCK		

[Table 35] DDR4-1866 Speed Bins and Operations

Speed Bin			DDR4-1866		Unit	Note	
CL-nRCD-nRP			13-13-13				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		13.92 ¹⁴⁾ (13.50) ^{5),12)}	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 2nCK	tAA(max) + 2nCK	ns	12	
ACT to internal read or write delay time	tRCD		13.92 ¹⁴⁾ (13.50) ^{5),12)}	-	ns	12	
PRE command period	tRP		13.92 ¹⁴⁾ (13.50) ^{5),12)}	-	ns	12	
ACT to PRE command period	tRAS		34	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		47.92 ¹⁴⁾ (47.50) ^{5),12)}	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional) ^{5),12)}	tCK(AVG)	1.5	1.6	ns	1,2,3,4,6,11
				(Optional) ^{5),12),14)}			
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,6,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
				(Optional) ^{5),12)}			
CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6	
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings			(9),(11),12,13,14		nCK	13,14	
Supported CL Settings with read DBI			(11),(13),14,15,16		nCK	13	
Supported CWL Settings			9,10,11,12		nCK		

[Table 36] DDR4-2133 Speed Bins and Operations

Speed Bin			DDR4-2133		Unit	Note	
CL-nRCD-nRP			15-15-15				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		14.06 ¹⁴⁾ (13.50) ^{9),12)}	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12	
ACT to internal read or write delay time	tRCD		14.06 ¹⁴⁾ (13.50) ^{5),12)}	-	ns	12	
PRE command period	tRP		14.06 ¹⁴⁾ (13.50) ^{5),12)}	-	ns	12	
ACT to PRE command period	tRAS		33	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		47.06 ¹⁴⁾ (47.50) ^{5),12)}	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11 (Optional) ^{5),12)}	tCK(AVG)	1.5 (Optional) ^{5),12),14)}	1.6	ns	1,2,3,4,7,11
			tCK(AVG)	Reserved			
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional) ^{5),12)}	<1.5	ns	1,2,3,4,6
			tCK(AVG)	1.25			
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071 (Optional) ^{5),12)}	<1.25	ns	1,2,3,4,7
			tCK(AVG)	1.071			
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
			tCK(AVG)	0.937	<1.071	ns	1,2,3,4
			tCK(AVG)	0.937	<1.071	ns	1,2,3
Supported CL Settings			(9),(11),12,(13),14,15,16		nCK	13,14	
Supported CL Settings with read DBI			(11),(13),14,(15),16,18,19		nCK	13	
Supported CWL Settings			9,10,11,12,14		nCK		

[Table 37] DDR4-2400 Speed Bins and Operations

Speed Bin			DDR4-2400		Unit	Note
CL-nRCD-nRP			17-17-17			
Parameter	Symbol		min	max		
Internal read command to first data	tAA		14.16 (13.50) ^{5),12)}	18.00	ns	12
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12
ACT to internal read or write delay time	tRCD		14.16 ¹⁴⁾ (13.75) ^{5),12)}	-	ns	12
PRE command period	tRP		14.16 ¹⁴⁾ (13.75) ^{5),12)}	-	ns	12
ACT to PRE command period	tRAS		32	9 x tREFI	ns	12
ACT to ACT or REF command period	tRC		46.16 ¹⁴⁾ (45.75) ^{5),12)}	-	ns	12
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11 (Optional) ^{5),12)}	tCK(AVG)	Reserved	ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5 1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25 <1.5 (Optional) ^{5),12)}	ns	1,2,3,4,8
	CL = 12	CL = 14	tCK(AVG)	1.25 <1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved	ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071 <1.25 (Optional) ^{5),12)}	ns	1,2,3,4,8
	CL = 14	CL = 16	tCK(AVG)	1.071 <1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved	ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937 <1.071 (Optional) ^{5),12)}	ns	1,2,3,4,8
	CL = 16	CL = 19	tCK(AVG)	0.937 <1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		
	CL = 16	CL = 19	tCK(AVG)	Reserved		
	CL = 17	CL = 20	tCK(AVG)	0.833 <0.937		
	CL = 18	CL = 21	tCK(AVG)	0.833 <0.937		
Supported CL Settings			10,(11),12,(13),14,(15),16,17,18		nCK	13
Supported CL Settings with read DBI			12,(13),14,(15),16,(18),19,20,21		nCK	13
Supported CWL Settings			9,10,11,12,14,16		nCK	

[Table 38] DDR4-2666 Speed Bins and Operations

Speed Bin			DDR4-2666		Unit	Note
CL-nRCD-nRP			19-19-19			
Parameter	Symbol		min	max		
Internal read command to first data	tAA		14.25 (13.50) ^(5),12)	18.00	ns	12
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 3nCK	tAA(max) + 3nCK	ns	12
ACT to internal read or write delay time	tRCD		14.25 (13.75) ^(5),12)	-	ns	12
PRE command period	tRP		14.25 (13.75) ^(5),12)	-	ns	12
ACT to PRE command period	tRAS		32	9 x tREFI	ns	12
ACT to ACT or REF command period	tRC		46.25 (45.75) ^(5),12)	-	ns	12
	Normal	Read DBI				
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved	ns	1,2,3,4,9,11
	CL = 10	CL = 12	tCK(AVG)	1.5 1.6	ns	1,2,3,9,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved	ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25 <1.5 (Optional) ^(5),12)	ns	1,2,3,4,9
	CL = 12	CL = 14	tCK(AVG)	1.25 <1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved	ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071 <1.25 (Optional) ^(5),12)	ns	1,2,3,4,9
	CL = 14	CL = 16	tCK(AVG)	1.071 <1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved	ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937 <1.071 (Optional) ^(5),12)	ns	1,2,3,4,9
	CL = 16	CL = 19	tCK(AVG)	0.937 <1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved	ns	1,2,3,9
	CL = 16	CL = 19	tCK(AVG)	Reserved	ns	4
	CL = 17	CL = 20	tCK(AVG)	0.833 <0.937 (Optional) ^(5),12)	ns	1,2,3,4,9
	CL = 18	CL = 21	tCK(AVG)	0.833 <0.937	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75 <0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75 <0.833	ns	1,2,3
Supported CL Settings			10,(11),12,(13),14,(15),16,(17),18,19,20		nCK	13
Supported CL Settings with read DBI			12,(13),14,(15),17,(18),19,(20),21,22,23		nCK	
Supported CWL Settings			9,10,11,12,14,16,18		nCK	

[Table 39] DDR4-2933 Speed Bins and Operations

Speed Bin			DDR4-2933		Unit	Note	
CL-nRCD-nRP			21-21-21				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		14.32 (13.75) ^(5),12)	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 4nCK	tAA(max) + 4nCK	ns	12	
ACT to internal read or write delay time	tRCD		14.32 (13.75) ^(5),12)	-	ns	12	
PRE command period	tRP		14.32 (13.75) ^(5),12)	-	ns	12	
ACT to PRE command period	tRAS		32	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		46.32 (45.75) ^(5),12)	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,11,15
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11,15
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
				(Optional) ^(5),12)			
CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,15	
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,15
				(Optional) ^(5),12)			
CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,15	
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,15
				(Optional) ^(5),12)			
CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,15	
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,15
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,15
				(Optional) ^(5),12)			
CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,15	
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,15
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,15
				(Optional) ^(5),12)			
CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,15	
CWL = 16,20	CL = 19	CL = 23	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 21	CL = 25	tCK(AVG)			ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)			ns	1,2,3
Supported CL Settings			10,(11),12,(13),14,(15),16,(17),18,(19),20,21,22		nCK	13	
Supported CL Settings with read DBI			12,(13),14,(15),16,(18),19,(20),21,(22),23,25,26		nCK	13	
Supported CWL Settings			9,10,11,12,14,16,18,20		nCK		

[Table 40] DDR4-3200 Speed Bins and Operations

Speed Bin			DDR4-3200		Unit	Note	
CL-nRCD-nRP			22-22-22				
Parameter	Symbol		min	max			
Internal read command to first data	tAA		13.75	18.00	ns	12	
Internal read command to first data with read DBI enabled	tAA_DBI		tAA(min) + 4nCK	tAA(max) + 4nCK	ns	12	
ACT to internal read or write delay time	tRCD		13.75	-	ns	12	
PRE command period	tRP		13.75	-	ns	12	
ACT to PRE command period	tRAS		32	9 x tREFI	ns	12	
ACT to ACT or REF command period	tRC		45.75	-	ns	12	
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,10,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,10,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,10
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,10
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,10
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,10
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,10
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,10
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,10
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,10
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,10
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,10
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 21	CL = 25	tCK(AVG)	0.682	<0.75	ns	1,2,3,4,10
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3,10
	CL = 24	CL = 28	tCK(AVG)	0.682	<0.75	ns	1,2,3,10
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	0.625	<0.682	ns	1,2,3,4
	CL = 24	CL = 28	tCK(AVG)	0.625	<0.682	ns	1,2,3
Supported CL Settings			10,(1,12,13,14,15,16,17,18,19,20,21,22,24		nCK		
Supported CL Settings with read DBI			12,13,14,15,16,18,19,20,21,22,23,25,26,28		nCK		
Supported CWL Settings			9,10,11,12,14,16,18,20		nCK		

10.1 Speed Bin Table Note

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

- 1) The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
- 2) tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from tAA following rounding algorithm defined in Section 13.5.
- 3) tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071ns or 0.937ns or 0.833ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
- 4) 'Reserved' settings are not allowed. User must program a different value.
- 5) 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Any combination of the 'optional' CL's is supported. The associated 'optional' tAA, tRCD, tRP, and tRC values must be adjusted based upon the CL combination supported. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
- 6) Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
- 7) Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
- 8) Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
- 9) Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
- 10) Any DDR4-3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
- 11) DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
- 12) Parameters apply from tCK(avg) min to tCK(avg) max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
- 13) CL number in parentheses, it means that these numbers are optional.
- 14) DDR4 SDRAM supports CL=9 as long as a system meets tAA(min), tRCD(min), tRP(min), and tRC(min).
- 15) Any DDR4-2933 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
- 16) Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins
- 17) Any DDR4-1600 Speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.

11. IDD And IDDQ Specification Parameters And Test conditions

11.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 21 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 22. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as $V_{IN} \leq V_{ILAC}(max)$.
- “1” and “HIGH” is defined as $V_{IN} \geq V_{IHAC}(min)$.
- “MID-LEVEL” is defined as inputs are $V_{REF} = V_{DD} / 2$.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 41.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 43.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 44 through Table 51.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
 $RON = RZQ/7$ (34 Ohm in MR1);
 $RTT_NOM = RZQ/6$ (40 Ohm in MR1);
 $RTT_WR = RZQ/2$ (120 Ohm in MR2);
 $RTT_PARK = Disable$;
 $Qoff = 0B$ (Output Buffer enabled) in MR1
 $TDQS_t$ disabled in MR1;
 CRC disabled in MR2;
 CA parity feature disabled in MR5;
 Gear down mode disabled in MR3
 Read/Write DBI disabled in MR5;
 DM disabled in MR5
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define $D = \{CS_n, ACT_n, RAS_n, CAS_n, WE_n\} := \{HIGH, LOW, LOW, LOW, LOW\}$; apply BG/BA changes when directed.
- Define $D\# = \{CS_n, ACT_n, RAS_n, CAS_n, WE_n\} := \{HIGH, HIGH, HIGH, HIGH, HIGH\}$; apply invert of BG/BA changes when directed above.

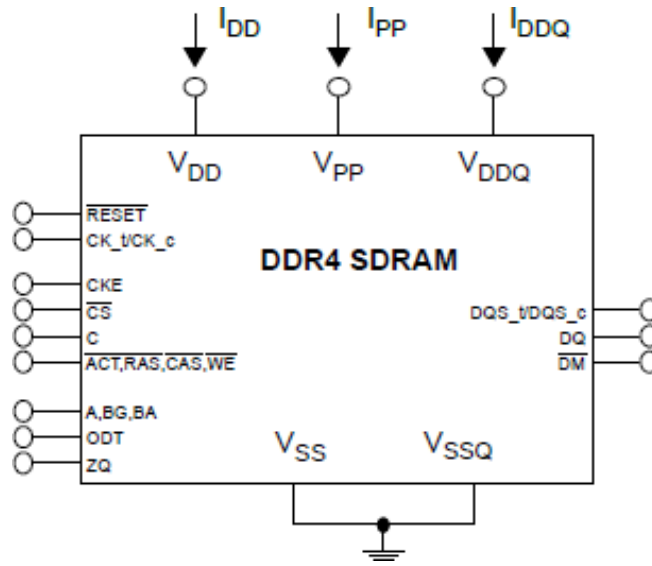


Figure 21. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

NOTE :

1) DIMM level Output test load condition may be different from above.

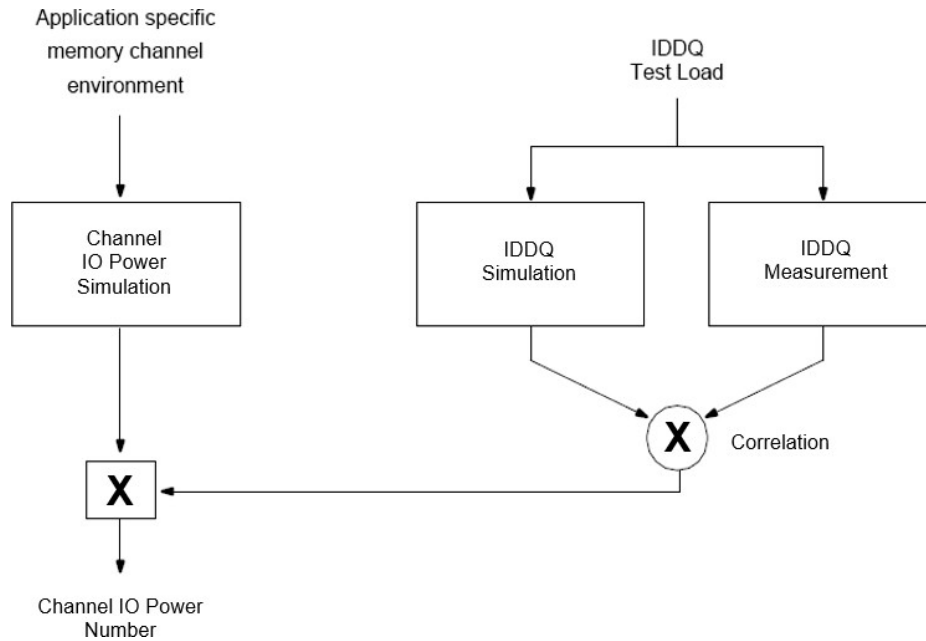


Figure 22. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

[Table 41] Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
		11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	21-21-21	22-22-22	
tCK		1.25	1.071	0.937	0.833	0.75	0.682	0.625	ns
CL		11	13	15	17	19	21	22	nCK
CWL		11	12	14	16	18	20	20	nCK
nRCD		11	13	15	17	19	21	22	nCK
nRC		39	45	51	56	62	68	74	nCK
nRAS		28	32	36	39	43	47	52	nCK
nRP		11	13	15	17	19	21	22	nCK
nFAW	x16	28	28	32	36	40	44	48	nCK
nRRDS	x16	5	6	6	7	8	8	9	nCK
nRRDL	x16	6	6	7	8	9	10	11	nCK
tCCD_S		4	4	4	4	4	4	4	nCK
tCCD_L		5	5	6	6	7	8	8	nCK
tWTR_S		2	3	3	3	4	4	4	nCK
tWTR_L		6	7	8	9	10	11	12	nCK
nRFC 2Gb		128	150	171	193	214	235	256	nCK
nRFC 4Gb		208	243	278	313	347	382	416	nCK
nRFC 8Gb		280	327	374	421	467	514	560	nCK

[Table 42] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 42; BL: 8 ¹ ; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 43; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 44); Output Buffer and RTT: Enabled in Mode Registers ²); ODT Signal: stable at 0; Pattern Details: see Table 43
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0
IPP0	Operating One Bank Active-Precharge IPP Current Same condition with IDD0
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 42; BL: 8 ¹ ; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling according to Table 44; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 44); Output Buffer and RTT: Enabled in Mode Registers ²); ODT Signal: stable at 0; Pattern Details: see Table 45
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1
IPP1	Operating One Bank Active-Read-Precharge IPP Current Same condition with IDD1
IDD2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: see Table 42; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 45; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²); ODT Signal: stable at 0; Pattern Details: see Table 46
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N
IPP2N	Precharge Standby IPP Current Same condition with IDD2N
IPP2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 42; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs, partially toggling according to Table 47; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²); ODT Signal: toggling according to Table 47; Pattern Details: see Table 47
IDDQ2NT (Optional)	Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled ³)
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled ^{3,5})
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled ³)
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled ³)
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 41; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²); ODT Signal: stable at 0
IPP2P	Precharge Power-Down IPP Current Same condition with IDD2P
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 42; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²); ODT Signal: stable at 0
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 42; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 45; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ²); ODT Signal: stable at 0; Pattern Details: see Table 46
IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N

Table 42] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IPP3N	Active Standby IPP Current Same condition with IDD3N
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 42; BL: 8 ¹⁾ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0
IPP3P	Active Power-Down IPP Current Same condition with IDD3P
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 42; BL: 8 ¹⁾ ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 48; Data IO: seamless read data burst with different data between one burst and the next one according to Table 48; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 48); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see table 48
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled ³⁾ , Other conditions: see IDD4R
IPP4R	Operating Burst Read IPP Current Same condition with IDD4R
IDDQ4R (Optional)	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	Operating Burst Read IDDQ Current with Read DBI Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 42; BL: 8 ¹⁾ ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 49; Data IO: seamless write data burst with different data between one burst and the next one according to Table 49; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 49); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at HIGH; Pattern Details: see table 49
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled ³⁾ , Other conditions: see IDD4W
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled ³⁾ , Other conditions: see IDD4W
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled ³⁾ , Other conditions: see IDD4W
IPP4W	Operating Burst Write IPP Current Same condition with IDD4W
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: see Table 41; BL: 8 ¹⁾ ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling according to Table 51; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC (see Table 50); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 51
IPP5B	Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B
IPP5F2	Burst Refresh Write IPP Current (2X REF) Same condition with IDD5F2
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B
IPP5F4	Burst Refresh Write IPP Current (4X REF) Same condition with IDD5F4

Table 42] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD6N	Self Refresh Current: Normal Temperature Range <i>T</i> _{CASE} for CT devices: 0 to 85°C, <i>T</i> _{CASE} for IT devices: -40 to 85°C; Low Power Auto Self Refresh (LP ASR) : Normal ⁴⁾ ; CKE : Low; External clock : Off; CK_t and CK_{c#} : LOW; CL : see Table 41; BL : 8 ¹⁾ ; AL : 0; CS_{n#} , Command , Address , Bank Group Address , Bank Address , Data IO : High; DM_n : stable at 1; Bank Activity : Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ²⁾ ; ODT Signal : MID-LEVEL
IPP6N	Self Refresh IPP Current: Normal Temperature Range Same condition with IDD6N
IDD6E	Self-Refresh Current: Extended Temperature Range <i>T</i> _{CASE} for CT devices: 0 to 95°C, <i>T</i> _{CASE} for IT devices: -40 to 95°C; Low Power Auto Self Refresh (LP ASR) : Extended ⁴⁾ ; CKE : Low; External clock : Off; CK_t and CK_{c#} : LOW; CL : see Table 41; BL : 8 ¹⁾ ; AL : 0; CS_n , Command , Address , Bank Group Address , Bank Address , Data IO : High; DM_n : stable at 1; Bank Activity : Extended Temperature Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ²⁾ ; ODT Signal : MID-LEVEL
IPP6E	Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E
IDD6R	Self-Refresh Current: Reduced Temperature Range <i>T</i> _{CASE} for CT devices: 0 to 45°C, <i>T</i> _{CASE} for IT devices: -40 to 85°C; Low Power Auto Self Refresh (LP ASR) : Reduced ⁴⁾ ; CKE : Low; External clock : Off; CK_t and CK_{c#} : LOW; CL : see Table 41; BL : 8 ¹⁾ ; AL : 0; CS_{n#} , Command , Address , Bank Group Address , Bank Address , Data IO : High; DM_n : stable at 1; Bank Activity : Extended Temperature Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ²⁾ ; ODT Signal : MID-LEVEL
IPP6R	Self Refresh IPP Current: Reduced Temperature Range Same condition with IDD6R
IDD6A	Auto Self-Refresh Current <i>T</i> _{CASE} for CT devices: 0 to 95°C, <i>T</i> _{CASE} for IT devices: -40 to 95°C; Low Power Auto Self Refresh (LP ASR) : Auto ⁴⁾ ; CKE : Low; External clock : Off; CK_t and CK_{c#} : LOW; CL : see Table 41; BL : 8 ¹⁾ ; AL : 0; CS_{n#} , Command , Address , Bank Group Address , Bank Address , Data IO : High; DM_n : stable at 1; Bank Activity : Auto Self-Refresh operation; Output Buffer and RTT : Enabled in Mode Registers ²⁾ ; ODT Signal : MID-LEVEL
IPP6A	Auto Self-Refresh IPP Current Same condition with IDD6A
IDD7	Operating Bank Interleave Read Current CKE : High; External clock : On; tCK , nRC , nRAS , nRCD , nRRD , nFAW , CL : see table 42: BL :8 ¹⁾ ; AL : CL-1; CS_n : High between ACT and RDA; Command , Address , Bank Group Address , Bank Group Address , Bank Address Inputs : Partially toggling according to Table 52; Data IO : read data bursts with different data between one burst and the next one according to Table 52; DM_n : stable at 1; Bank Activity : two times interleaved cycling through banks (0, 1, ...,7) with different addressing, see Table 52; Output Buffer and RTT : Enabled in mode Registers ²⁾ ; ODT Signal : stable at 0; Pattern Details : see Table 52
IPP7	Operating Bank Interleave Read IPP Current Same condition with IDD7
IDD8	Maximum Power Down Current Place DRAM in MPSM
IPP8	Maximum Power Down IPP Current Same condition with IDD8

NOTE:

- 1) Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
- 2) Output Buffer Enable
 - set MR1 [A12 = 0]: Qoff = Output buffer enabled
 - set MR1 [A2:1 = 00]: Output Driver Impedance Control = RZQ/7
 - RTT_{Nom} enable
 - set MR1 [A10:8 = 011]: RTT_{NOM} = RZQ/6
 - RTT_{WR} enable
 - set MR2 [A10:9 = 01]: RTT_{WR} = RZQ/2
 - RTT_{PARK} disable
 - set MR5 [A8:6 = 000]
- 3) CAL enabled: set MR4 [A8:6 = 001]: 1600MT/s
 - 010]: 1866MT/s,2133MT/s
 - 011]: 2400MT/s,2666MT/s
 - 100]: 2933MT/s,3200MT/s
 Gear Down mode enabled: set MR3 [A3 = 1]: 1/4 Rate
 DLL disabled: set MR1 [A0 = 0]
 CA parity enabled: set MR5 [A2:0 = 001]: 1600MT/s,1866MT/s, 2133MT/s
 - 010]: 2400MT/s,2666MT/s
 - 011]: 2933MT/s,3200MT/s
 Read DBI enabled: set MR5 [A12 = 1]
 Write DBI enabled: set MR5 [A11 = 1]
- 4) Low Power Array Self Refresh (LP ASR): set MR2 [A7:6 = 00]: Normal
 - 01]: Reduced Temperature range
 - 10]: Extended Temperature range
 - 11]: Auto Self Refresh
- 5) IDD2NG should be measured after sync pulses (NOP) input.

[Table 43] IDD0, IDD0A and IPP0 Measurement-Loop Pattern ¹⁾

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³⁾	BG[1:0] ²⁾	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴⁾			
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D_#, D_#	1	1	1	1	1	1	0	0	0	3 ²⁾	3	0	0	0	7	F	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																			
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																			
		1	1*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 1, BA[1:0] = 1 instead																			
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 2 instead																			
		3	3*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 1, BA[1:0] = 3 instead																			
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 1 instead																			
		5	5*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 1, BA[1:0] = 2 instead																			
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 3 instead																			
		7	7*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 1, BA[1:0] = 0 instead																			
		8	8*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 0 instead																			
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 3, BA[1:0] = 1 instead																			
10	10*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 2 instead																					
11	11*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 3, BA[1:0] = 3 instead																					
12	12*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 1 instead																					
13	13*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 3, BA[1:0] = 2 instead																					
14	14*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 3 instead																					
15	15*nRC	repeat Sub-Loop 0, use BG[1:0]²⁾ = 3, BA[1:0] = 0 instead																					

NOTE:

- 1) DQS_t, DQS_c are VDDQ.
- 2) BG1 is don't care for x16 device
- 3) C[2:0] are used only for 3DS device
- 4) DQ signals are VDDQ.

[Table 44] IDD1, IDD1A and IPP1 Measurement-Loop Pattern¹

CK_t/CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³⁾	BG[1:0] ²⁾	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴⁾			
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3,4	D_#, D_#	1	1	1	1	1	1	0	0	3b)	3	0	0	0	7	F	0	0	-	
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																			
			nRCD -AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																			
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																			
		1	1*nRC + 0	ACT	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	1	0	0	3b)	3	0	0	0	7	F	0	0		
			...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																			
			1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																			
			1*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	
			...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																			
		2	2*nRC	repeat Sub-Loop 0, use BG[1:0] ²⁾ = 0, BA[1:0] = 2 instead																			
		3	3*nRC	repeat Sub-Loop 1, use BG[1:0] ²⁾ = 1, BA[1:0] = 3 instead																			
		4	4*nRC	repeat Sub-Loop 0, use BG[1:0] ²⁾ = 0, BA[1:0] = 1 instead																			
		5	5*nRC	repeat Sub-Loop 1, use BG[1:0] ²⁾ = 1, BA[1:0] = 2 instead																			
		6	6*nRC	repeat Sub-Loop 0, use BG[1:0] ²⁾ = 0, BA[1:0] = 3 instead																			
		7	7*nRC	repeat Sub-Loop 1, use BG[1:0] ²⁾ = 1, BA[1:0] = 0 instead																			
		8	8*nRC	repeat Sub-Loop 1, use BG[1:0] ²⁾ = 2, BA[1:0] = 0 instead																			
		9	9*nRC	repeat Sub-Loop 0, use BG[1:0] ²⁾ = 3, BA[1:0] = 1 instead																			
		10	10*nRC	repeat Sub-Loop 1, use BG[1:0] ²⁾ = 2, BA[1:0] = 2 instead																			
		11	11*nRC	repeat Sub-Loop 0, use BG[1:0] ²⁾ = 3, BA[1:0] = 3 instead																			
		12	12*nRC	repeat Sub-Loop 1, use BG[1:0] ²⁾ = 2, BA[1:0] = 1 instead																			
		13	13*nRC	repeat Sub-Loop 0, use BG[1:0] ²⁾ = 3, BA[1:0] = 2 instead																			
14	14*nRC	repeat Sub-Loop 1, use BG[1:0] ²⁾ = 2, BA[1:0] = 3 instead																					
15	15*nRC	repeat Sub-Loop 0, use BG[1:0] ²⁾ = 3, BA[1:0] = 0 instead																					

NOTE :

- 1) DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
- 2) BG1 is don't care for x16 device.
- 3) C[2:0] are used only for 3DS device.
- 4) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

[Table 45] IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2, IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern¹⁾

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³⁾	BG[1:0] ²⁾	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴⁾		
togglin	Static	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D#, D#	1	1	1	1	1	1	0	0	3 ²⁾	3	0	0	0	7	F	0	0	0
			3	D#, D#	1	1	1	1	1	1	0	0	3 ²⁾	3	0	0	0	7	F	0	0	0
		1	4-7	repeat Sub-Loop 0, use BG[1:0]²⁾ = 1, BA[1:0] = 1 instead																		
		2	8-11	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 2 instead																		
		3	12-15	repeat Sub-Loop 0, use BG[1:0]²⁾ = 1, BA[1:0] = 3 instead																		
		4	16-19	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 1 instead																		
		5	20-23	repeat Sub-Loop 0, use BG[1:0]²⁾ = 1, BA[1:0] = 2 instead																		
		6	24-27	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 3 instead																		
		7	28-31	repeat Sub-Loop 0, use BG[1:0]²⁾ = 1, BA[1:0] = 0 instead																		
		8	32-35	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 0 instead																		
		9	36-39	repeat Sub-Loop 0, use BG[1:0]²⁾ = 3, BA[1:0] = 1 instead																		
		10	40-43	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 2 instead																		
		11	44-47	repeat Sub-Loop 0, use BG[1:0]²⁾ = 3, BA[1:0] = 3 instead																		
		12	48-51	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 1 instead																		
13	52-55	repeat Sub-Loop 0, use BG[1:0]²⁾ = 3, BA[1:0] = 2 instead																				
14	56-59	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 3 instead																				
15	60-63	repeat Sub-Loop 0, use BG[1:0]²⁾ = 3, BA[1:0] = 0 instead																				

NOTE :

- 1) DQS_t, DQS_c are VDDQ.
- 2) BG1 is don't care for x16 device.
- 3) C[2:0] are used only for 3DS device.
- 4) DQ signals are VDDQ.

[Table 46] IDD2NT and IDDQ2NT Measurement-Loop Pattern¹⁾

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³⁾	BG[1:0] ²⁾	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴⁾		
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D#, D#	1	1	1	1	1	1	0	0	3 ²⁾	3	0	0	0	7	F	0	0	-
			3	D#, D#	1	1	1	1	1	1	0	0	3 ²⁾	3	0	0	0	7	F	0	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and $BG[1:0]^2) = 1$, $BA[1:0] = 1$ instead																		
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and $BG[1:0]^2) = 0$, $BA[1:0] = 2$ instead																		
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and $BG[1:0]^2) = 1$, $BA[1:0] = 3$ instead																		
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and $BG[1:0]^2) = 0$, $BA[1:0] = 1$ instead																		
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and $BG[1:0]^2) = 1$, $BA[1:0] = 2$ instead																		
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and $BG[1:0]^2) = 0$, $BA[1:0] = 3$ instead																		
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and $BG[1:0]^2) = 1$, $BA[1:0] = 0$ instead																		
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and $BG[1:0]^2) = 2$, $BA[1:0] = 0$ instead																		
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and $BG[1:0]^2) = 3$, $BA[1:0] = 1$ instead																		
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and $BG[1:0]^2) = 2$, $BA[1:0] = 2$ instead																		
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and $BG[1:0]^2) = 3$, $BA[1:0] = 3$ instead																		
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and $BG[1:0]^2) = 2$, $BA[1:0] = 1$ instead																		
13	52-55	repeat Sub-Loop 0, but ODT = 1 and $BG[1:0]^2) = 3$, $BA[1:0] = 2$ instead																				
14	56-59	repeat Sub-Loop 0, but ODT = 0 and $BG[1:0]^2) = 2$, $BA[1:0] = 3$ instead																				
15	60-63	repeat Sub-Loop 0, but ODT = 1 and $BG[1:0]^2) = 3$, $BA[1:0] = 0$ instead																				

For x4 and x8 only

- NOTE :**
- 1) DQS_t, DQS_c are VDDQ.
 - 2) BG1 is don't care for x16 device.
 - 3) C[2:0] are used only for 3DS device.
 - 4) DQ signals are VDDQ.

[Table 47] IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern¹⁾

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³⁾	BG[1:0] ²⁾	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴⁾		
toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2,3	D#, D#	1	1	1	1	1	1	0	0	0	3 ²⁾	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	0	1	1	0	0	0	7	F	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	0	0	3 ²⁾	3	0	0	0	7	F	0	-
		2	8-11	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 2 instead																		
		3	12-15	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 3 instead																		
		4	16-19	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 1 instead																		
		5	20-23	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 2 instead																		
		6	24-27	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 3 instead																		
		7	28-31	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 0 instead																		
		8	32-35	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 0 instead																		
		9	36-39	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 1 instead																		
		10	40-43	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 2 instead																		
11	44-47	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 3 instead																				
12	48-51	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 1 instead																				
13	52-55	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 2 instead																				
14	56-59	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 3 instead																				
15	60-63	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 0 instead																				
																				For x4 and x8 only		

NOTE :

- 1) DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
- 2) BG1 is don't care for x16 device.
- 3) C[2:0] are used only for 3DS device.
- 4) Burst Sequence driven on each DQ signal by Read Command.

[Table 48] IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern¹⁾

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³⁾	BG[1:0] ²⁾	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴⁾		
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
			1	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			2,3	D#, D#	1	1	1	1	1	1	1	0	3 ²⁾	3	0	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	0	0	1	0	1	1	0	0	0	7	F	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00
			5	D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			6,7	D#, D#	1	1	1	1	1	1	1	0	3 ²⁾	3	0	0	0	7	F	0	-	
		2	8-11	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 2 instead																		
		3	12-15	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 3 instead																		
		4	16-19	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 1 instead																		
		5	20-23	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 2 instead																		
		6	24-27	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 3 instead																		
		7	28-31	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 0 instead																		
		8	32-35	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 0 instead																		
		9	36-39	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 1 instead																		
		10	40-43	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 2 instead																		
11	44-47	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 3 instead																				
12	48-51	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 1 instead																				
13	52-55	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 2 instead																				
14	56-59	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 3 instead																				
15	60-63	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 0 instead																				
																				For x4 and x8 only		

NOTE :

- 1) DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
- 2) BG1 is don't care for x16 device.
- 3) C[2:0] are used only for 3DS device.
- 4) Burst Sequence driven on each DQ signal by Write Command.

[Table 49] IDD4WC Measurement-Loop Pattern¹⁾

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³⁾	BG[1:0] ²⁾	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴⁾		
toggling	Static High	0	0	WR	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC	
			1,2	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D#, D#	1	1	1	1	1	1	1	0	3 ²⁾	3	0	0	0	0	7	F	0	-
		1	5	WR	0	1	1	0	0	0	1	0	1	1	0	0	0	7	F	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC
			6,7	D, D	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			8,9	D#, D#	1	1	1	1	1	1	1	0	3 ²⁾	3	0	0	0	7	F	0	-	
		2	10-14	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 2 instead																		
		3	15-19	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 3 instead																		
		4	20-24	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 1 instead																		
		5	25-29	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 2 instead																		
		6	30-34	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 3 instead																		
		7	35-39	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 0 instead																		
		8	40-44	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 0 instead																		
		9	45-49	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 1 instead																		
		10	50-54	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 2 instead																		
11	55-59	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 3 instead																				
12	60-64	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 1 instead																				
13	65-69	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 2 instead																				
14	70-74	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 3 instead																				
15	75-79	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 0 instead																				
																				For x4 and x8 only		

NOTE :

- 1) DQS_t, DQS_c are VDDQ.
- 2) BG1 is don't care for x16 device.
- 3) C[2:0] are used only for 3DS device.
- 4) Burst Sequence driven on each DQ signal by Write Command.

[Table 50] IDD5B Measurement-Loop Pattern¹⁾

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³⁾	BG[1:0] ²⁾	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴⁾		
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		2	2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		3	3	D#, D#	1	1	1	1	1	1	0	0	3 ²⁾	3	0	0	0	7	F	0	0	-
		4	4	D#, D#	1	1	1	1	1	1	0	0	3 ²⁾	3	0	0	0	7	F	0	0	-
		5-8	repeat pattern 1...4, use BG[1:0]²⁾ = 1, BA[1:0] = 1 instead																			
		9-11	repeat pattern 1...4, use BG[1:0]²⁾ = 0, BA[1:0] = 2 instead																			
		12-15	repeat pattern 1...4, use BG[1:0]²⁾ = 1, BA[1:0] = 3 instead																			
		16-19	repeat pattern 1...4, use BG[1:0]²⁾ = 0, BA[1:0] = 1 instead																			
		20-23	repeat pattern 1...4, use BG[1:0]²⁾ = 1, BA[1:0] = 2 instead																			
		24-27	repeat pattern 1...4, use BG[1:0]²⁾ = 0, BA[1:0] = 3 instead																			
		28-31	repeat pattern 1...4, use BG[1:0]²⁾ = 1, BA[1:0] = 0 instead																			
		32-35	repeat pattern 1...4, use BG[1:0]²⁾ = 2, BA[1:0] = 0 instead																			
		36-39	repeat pattern 1...4, use BG[1:0]²⁾ = 3, BA[1:0] = 1 instead																			
		40-43	repeat pattern 1...4, use BG[1:0]²⁾ = 2, BA[1:0] = 2 instead																			
		44-47	repeat pattern 1...4, use BG[1:0]²⁾ = 3, BA[1:0] = 3 instead																			
		48-51	repeat pattern 1...4, use BG[1:0]²⁾ = 2, BA[1:0] = 1 instead																			
		52-55	repeat pattern 1...4, use BG[1:0]²⁾ = 3, BA[1:0] = 2 instead																			
		56-59	repeat pattern 1...4, use BG[1:0]²⁾ = 2, BA[1:0] = 3 instead																			
		60-63	repeat pattern 1...4, use BG[1:0]²⁾ = 3, BA[1:0] = 0 instead																			
2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																				

- NOTE :**
- 1) DQS_t, DQS_c are VDDQ.
 - 2) BG1 is don't care for x16 device.
 - 3) C[2:0] are used only for 3DS device.
 - 4) DQ signals are VDDQ.

[Table 51] IDD7 Measurement-Loop Pattern¹⁾

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0] ³⁾	BG[1:0] ²⁾	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴⁾			
toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1	RDA	0	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF	
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3	D#	1	1	1	1	1	1	0	0	3 ²⁾	3	0	0	0	0	7	F	0	-	
			...	repeat pattern 2...3 until nRRD - 1, if nRRD > 4. Truncate if necessary																			
		1	nRRD	ACT	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	-	
			nRRD + 1	RDA	0	1	1	0	1	0	0	0	1	1	0	0	1	0	0	0	0	D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00	
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRRD > 4. Truncate if necessary																			
		2	2*nRRD	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 2 instead																			
		3	3*nRRD	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 3 instead																			
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRRD. Truncate if necessary																			
		5	nFAW	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 1 instead																			
		6	nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 2 instead																			
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]²⁾ = 0, BA[1:0] = 3 instead																			
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]²⁾ = 1, BA[1:0] = 0 instead																			
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																			
		10	2*nFAW	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 0 instead																			
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 1 instead																			
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 2 instead																			
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 3 instead																			
14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																					
15	3*nFAW	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 1 instead																					
16	3*nFAW + nRRD	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 2 instead																					
17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use BG[1:0]²⁾ = 2, BA[1:0] = 3 instead																					
18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use BG[1:0]²⁾ = 3, BA[1:0] = 0 instead																					
19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																					
20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																					

NOTE:

- 1) DQS_t, DQS_c are VDDQ.
- 2) BG1 is don't care for x16 device.
- 3) C[2:0] are used only for 3DS device.
- 4) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ

12. 8Gb DDR4 SDRAM IDD SPECIFICATION TABLE

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

[Table 52] I_{DD} and I_{DDQ} Specification

Symbol	512Mx16		Unit
	DDR4-2933	DDR4-3200	
	21-21-21	22-22-22	
	VDD 1.2V	VDD 1.2V	
	IDD Max.	IDD Max.	
I_{DD0}	46	47	mA
I_{DD0A}	50	51	mA
I_{DD1}	70	71	mA
I_{DD1A}	86	86	mA
I_{DD2N}	22	23	mA
I_{DD2NA}	28	28	mA
I_{DD2NT}	30	30	mA
I_{DD2NL}	14	17	mA
I_{DD2NG}	23	24	mA
I_{DD2ND}	21	21	mA
I_{DD2N_par}	25	26	mA
I_{DD2P}	13	14	mA
I_{DD2Q}	19	21	mA
I_{DD3N}	36	38	mA
I_{DD3NA}	30	38	mA
I_{DD3P}	20	21	mA
I_{DD4R}	223	243	mA
I_{DD4RA}	228	248	mA
I_{DD4RB}	222	240	mA
I_{DD4W}	158	172	mA
I_{DD4WA}	167	181	mA
I_{DD4WB}	159	173	mA
I_{DD4WC}	145	157	mA
I_{DD4W_par}	170	184	mA
I_{DD5B}	235	235	mA
I_{DD5F2}	165	165	mA
I_{DD5F4}	148	148	mA
I_{DD6N}	22	22	mA
I_{DD6E}	34	34	mA
I_{DD6R}	15	15	mA
I_{DD6A}	22	22	mA
I_{DD7}	293	296	mA
I_{DD8}	11	11	mA

[Table 53] I_{PP} Specification

Symbol	512Mx16		Unit
	DDR4-2933	DDR4-3200	
	21-21-21	22-22-22	
	VPP 2.5V	VPP 2.5V	
	IPP Max.	IPP Max.	
I _{PP0}	4	4	mA
I _{PP1}	4	4	mA
I _{PP2N}	3	3	mA
I _{PP2P}	3	3	mA
I _{PP3N}	4	4	mA
I _{PP3P}	4	4	mA
I _{PP4R}	4	4	mA
I _{PP4W}	4	4	mA
I _{PP5B}	25	25	mA
I _{PP5F2}	18	18	mA
I _{PP5F4}	17	17	mA
I _{PP6N}	4	4	mA
I _{PP6E}	5	5	mA
I _{PP6R}	4	4	mA
I _{PP6A}	4	4	mA
I _{PP7}	16	16	mA
I _{PP8}	3	3	mA

[Table 54] I_{DD6} Specification

Symbol	Temperature Range	512Mx16		Unit	Note
		DDR4-2933	DDR4-3200		
		21-21-21	22-22-22		
		VDD 1.2V	VDD 1.2V		
I _{DD6N}	0 - 85 °C	22	22	mA	1,2
I _{DD6E}	0 - 95 °C	33	33	mA	2,3

- NOTE :**
- 1) Applicable for MR2 settings A6=0 and A7=0.
 - 2) Supplier data sheets include a max value for I_{DD6}.
 - 3) Applicable for MR2 settings A6=0 and A7=1. I_{DD6ET} is only specified for devices which support the Extended Temperature Range feature.

5. INPUT/OUTPUT CAPACITANCE

[Table 55] Silicon Pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933		DDR4-3200		Unit	Note
		min	max	min	max	min	max	min	max		
C _{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	0.55	1.0	0.55	1.0	pF	1,2,3
C _{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C _{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	-	0.05	-	0.05	pF	1,2,3,5
C _{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	0.2	0.7	0.2	0.7	pF	1,3
C _{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	-	0.05	-	0.05	pF	1,3,4
C _I	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	0.2	0.6	0.2	0.55	pF	1,3,6
C _{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
C _{DI_ADD_CMD}	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C _{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	pF	1,3
C _{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	-	2.3	-	2.3	pF	1,3,12
C _{TEN}	Input capacitance of TEN	0.2	2.3	0.2	2.3	0.2	2.3	0.2	2.3	pF	1,3,13

NOTE :

- 1) This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating
- 2) DQ, DM_n, DQS_t, DQS_c, TDQS_c. Although the DM, TDQS_t and TDQS_c pins have different functions, the loading matches DQ and DQS
- 3) This parameter applies to monolithic devices only: stacked/dual-die devices are not covered here
- 4) Absolute value CK-t-CK_c
- 5) Absolute value of CIO(DQS_t)-CIO(DQS_c)
- 6) C_I applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
- 7) C_{DI_CTRL} applies to ODT, CS_n and CKE
- 8) C_{DI_CTRL} = C_I(CTRL)-0.5*(C_I(CK_t)+C_I(CK_c))
- 9) C_{DI_ADD_CMD} applies to, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
- 10) C_{DI_ADD_CMD} = C_I(ADD_CMD)-0.5*(C_I(CK_t)+C_I(CK_c))
- 11) C_{DIO} = C_{IO}(DQ,DM)-0.5*(C_{IO}(DQS_t)+C_{IO}(DQS_c))
- 12) Maximum external load capacitance on ZQ pin: 5 pF.
- 13) TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case C_{TEN} might not be valid and system shall verify TEN signal with Vendor specific information.

[Table 56] DRAM package electrical specifications (X16)

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200		Unit	Note
		min	max		
Z _{IO}	Input/output Zpkg	45	85	Ω	1
T _{diO}	Input/output Pkg Delay	14	45	ps	1
L _{io}	Input/Output Lpkg	-	3.4	nH	1, 2
C _{io}	Input/Output Cpkg	-	0.82	pF	1, 3
Z _{IO DQS}	DQS_t, DQS_c Zpkg	45	85	Ω	1
T _{diO DQS}	DQS_t, DQS_c Pkg Delay	14	45	ps	1
L _{io DQS}	DQS Lpkg	-	3.4	nH	1, 2
C _{io DQS}	DQS Cpkg	-	0.82	pF	1, 3
DZ _{DIO DQS}	Delta Zpkg DQSU_t, DQSU_c	-	10	Ω	-
	Delta Zpkg DQSL_t, DQSL_c	-	10	Ω	-
D _{TdDIO DQS}	Delta Delay DQSU_t, DQSU_c	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	ps	-
Z _{I CTRL}	Input CTRL pins Zpkg	50	90	Ω	1
T _{di_CTRL}	Input CTRL pins Pkg Delay	14	42	ps	1
L _{i CTRL}	Input CTRL Lpkg	-	3.4	nH	1, 2
C _{i CTRL}	Input CTRL Cpkg	-	0.7	pF	1, 3
Z _{IADD CMD}	Input- CMD ADD pins Zpkg	50	90	Ω	1
T _{diADD_CMD}	Input- CMD ADD pins Pkg Delay	14	52	ps	1
L _{i ADD CMD}	Input- CMD ADD Lpkg	-	3.9	nH	1, 2
C _{i ADD CMD}	Input- CMD ADD Cpkg	-	0.86	pF	1, 3
Z _{CK}	CK_t & CK_c Zpkg	50	90	Ω	1
T _{dCK}	CK_t & CK_c Pkg Delay	14	42	ps	1
L _{i CLK}	Input CK Lpkg	-	3.4	nH	1, 2
C _{i CLK}	Input CK Cpkg	-	0.7	pF	1, 3
DZ _{DCK}	Delta Zpkg CK_t & CK_c	-	10	Ω	-
D _{TdCK}	Delta Delay CK_t & CK_c	-	5	ps	-
Z _{OZQ}	ZQ Zpkg	-	100	Ω	-
T _{dO ZQ}	ZQ Delay	20	90	ps	-
Z _{O ALERT}	ALERT Zpkg	40	100	Ω	-
T _{dO ALERT}	ALERT Delay	20	55	ps	-

NOTE :

- 1) Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown
- 2) It is assumed that Lpkg can be approximated as $L_{pkg} = Z_o * T_d$
- 3) It is assumed that Cpkg can be approximated as $C_{pkg} = T_d / Z_o$

14. Electrical Characteristics & AC Timing

14.1 Reference Load for AC Timing and Output Slew Rate

Figure 23 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

Ron nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

The maximum DC High level of Output signal = $1.0 * VDDQ$,

The minimum DC Low level of Output signal = $\{34 / (34 + 50)\} * VDDQ = 0.4 * VDDQ$

The nominal reference level of an Output signal can be approximated by the following:

The center of maximum DC High and minimum DC Low = $\{(1 + 0.4) / 2\} * VDDQ = 0.7 * VDDQ$

The actual reference level of Output signal might vary with driver Ron and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment, or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics

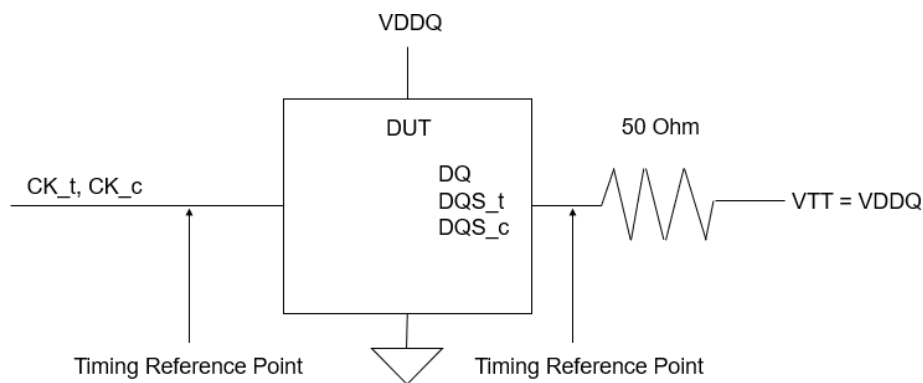


Figure 23. Reference Load for AC Timing and Output Slew Rate

14.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

[Table 57] tREFI by device density

Parameter	Symbol	2Gb	4Gb	8Gb	Units	Note
Average periodic refresh interval	tREFI	$0\text{ }^{\circ}\text{C} \leq T_{\text{CASE}} \leq 85\text{ }^{\circ}\text{C}$	7.8	7.8	7.8	μs
		$85\text{ }^{\circ}\text{C} < T_{\text{CASE}} \leq 95\text{ }^{\circ}\text{C}$	3.9	3.9	3.9	μs

14.3 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

14.3.1 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

14.3.2 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^N tCK(abs)_j \right) / N \quad N = 200$$

14.3.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^N tCH_j \right) / \{ N \times tCK(avg) \} \quad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^N tCL_j \right) / \{ N \times tCK(avg) \} \quad N = 200$$

14.3.4 Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test

15. TIMING PARAMETERS BY SPEED GRADE

[Table 58] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-3200

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing																	
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	0.750	<0.833	0.682	<0.750	0.625	<0.682	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	MIN : tCK(avg)min + tJIT(per)min_tot MAX : tCK(avg)max + tJIT(per)max_tot														tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	tJIT(per)_tot	-63	63	-54	54	-47	47	-42	42	-38	38	-34	34	-32	32	ps	23
Clock Period Jitter- deterministic	tJIT(per)_dj	-31	31	-27	27	-23	23	-21	21	-19	19	-17	17	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT(per)_lck	-50	50	-43	43	-38	38	-33	33	-30	30	-27	27	-25	25	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	125	-	107	-	94	-	83	-	75	-	68	-	62	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc)_lck	-	100	-	86	-	75	-	67	-	60	-	55	-	50	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	-55	55	-50	50	-46	46	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	-66	66	-60	60	-55	55	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	-73	73	-66	66	-61	61	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	-78	78	-71	71	-65	65	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	-83	83	-75	75	-69	69	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	-87	87	-79	79	-73	73	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	-91	91	-83	83	-76	76	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	-94	94	-85	85	-78	78	ps	
Cumulative error across 10 cycle	tERR(10per)	-169	160	-137	137	-120	120	-107	107	-96	96	-88	88	-80	80	ps	
Cumulative error across 11 cycle	tERR(11per)	-164	164	-141	141	-123	123	-110	110	-99	99	-90	90	-83	83	ps	
Cumulative error across 12 cycle	tERR(12per)	-168	168	-144	144	-126	126	-112	112	-101	101	-92	92	-84	84	ps	
Cumulative error across 13 cycle	tERR(13per)	-172	172	-147	147	-129	129	-114	114	-103	103	-93	93	-86	86	ps	
Cumulative error across 14 cycle	tERR(14per)	-175	175	-150	150	-131	131	-116	116	-104	104	-95	95	-87	87	ps	
Cumulative error across 15 cycle	tERR(15per)	-178	178	-152	152	-133	133	-118	118	-106	106	-97	97	-89	89	ps	
Cumulative error across 16 cycle	tERR(16per)	-180	189	-155	155	-135	135	-120	120	-108	108	-98	98	-90	90	ps	
Cumulative error across 17 cycle	tERR(17per)	-183	183	-157	157	-137	137	-122	122	-110	110	-100	100	-92	92	ps	
Cumulative error across 18 cycle	tERR(18per)	-185	185	-159	159	-139	139	-124	124	-112	112	-101	101	-93	93	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	MIN : tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) MAX : tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)														ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	55	-	48	-	40	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	145	-	138	-	130	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	80	-	73	-	65	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	145	-	138	-	130	-	ps	
Control and Address input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	385	-	365	-	340	-	ps	
Command and Address Timing																	
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250ns)	-	max(5 nCK, 5.355ns)	-	max(5 nCK, 5.355ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	nCK	

[Table 58] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-3200

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CAS _n to CAS _n command de- lay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Com- mand delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nC K,6ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Com- mand delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nC K,5ns)	-	Max(4nC K,4.2ns)	-	Max(4nC K,3.7ns)	-	Max(4nC K,3.3ns)	-	Max(4nC K,3ns)	-	Max(4nC K,2.7ns)	-	Max(4nC K,2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Com- mand delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nC K,5ns)	-	Max(4nC K,4.2ns)	-	Max(4nC K,3.7ns)	-	Max(4nC K,3.3ns)	-	Max(4nC K,3ns)	-	Max(4nC K,2.7ns)	-	Max(4nC K,2.5ns)	-	nCK	34
ACTIVATE to ACTIVATE Com- mand delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nC K,7.5ns)	-	Max(4nC K,6.4ns)	-	Max(4nC K,6.4ns)	-	Max(4nC K,6.4ns)	-	Max(4nC K,6.4ns)	-	Max(4nC K,6.4ns)	-	Max(4nC K,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Com- mand delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nC K,6ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,4.9ns)	-	Max(4nC K,4.9ns)	-	Max(4nC K,4.9ns)	-	Max(4nC K,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Com- mand delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nC K,6ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,5.3ns)	-	Max(4nC K,4.9ns)	-	Max(4nC K,4.9ns)	-	Max(4nC K,4.9ns)	-	Max(4nC K,4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28n CK,35ns)	-	Max(28n CK,30ns)	-	Max(28n CK,30ns)	-	Max(28n CK,30ns)	-	Max(28n CK,30ns)	-	Max(28n CK,30ns)	-	Max(28n CK,30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20n CK,25ns)	-	Max(20n CK,23ns)	-	Max(20n CK,21ns)	-	Max(20n CK,21ns)	-	Max(20n CK,21ns)	-	Max(20n CK,21ns)	-	Max(20n CK,21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16n CK,20ns)	-	Max(16n CK,17ns)	-	Max(16n CK,15ns)	-	Max(16n CK,13ns)	-	Max(16n CK,12ns)	-	Max(16n CK,10.875ns)	-	Max(16n CK,10ns)	-	ns	34
Delay from start of internal write transaction to internal read com- mand for different bank group	tWTR_S	Max(2nC K,2.5ns)	-	Max(2nC K,2.5ns)	-	Max(2nC K,2.5ns)	-	Max(2nC K,2.5ns)	-	Max(2nC K,2.5ns)	-	Max(2nC K,2.5ns)	-	Max(2nC K,2.5ns)	-	ns	1,2,34
Delay from start of internal wr transaction to internal read com- ma for same bank group	tWTR_L	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	ns	1,34
Internal READ Command to PRECHARGE Command delay	tRTP	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	Max(4nC K,7.5ns)	-	ns	1,34
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (4nC,3.7 5ns)	-	tWR+max (5nC,3.7 5ns)	-	tWR+max (5nC,3.7 5ns)	-	tWR+max (5nC,3.7 5ns)	-	tWR+max (5nC,3.7 5ns)	-	tWR+max (5nC,3.7 5ns)	-	tWR+max (5nC,3.7 5ns)	-	ns	1,28
Delay from start of internal write transaction to internal read com- mand for different bank group with both CRC and DM enabled	tWTR_S+ RC_DM	tWTR_S+ max (4nC,3.7 5ns)	-	tWTR_S+ max (5nC,3.7 5ns)	-	tWTR_S+ max (5nC,3.7 5ns)	-	tWTR_S+ max (5nC,3.7 5ns)	-	tWTR_S+ max (5nC,3.7 5ns)	-	tWTR_S+ max (5nC,3.7 5ns)	-	tWTR_S+ max (5nC,3.7 5ns)	-	ns	2,29,34
Delay from start of internal write transaction to internal read com- mand for same bank group with both CRC and DM enabled	tWTR_L+ RC_DM	tWTR_L+ max (4nC,3.7 5ns)	-	tWTR_L+ max (5nC,3.7 5ns)	-	tWTR_L+ max (5nC,3.7 5ns)	-	tWTR_L+ max (5nC,3.7 5ns)	-	tWTR_L+ max (5nC,3.7 5ns)	-	tWTR_L+ max (5nC,3.7 5ns)	-	tWTR_L+ max (5nC,3.7 5ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	1024	-	1024	-	1024	-	nCK	
Mode Register Set command cy- cle time	tMRD	8	-	8	-	8	-	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command up- date delay	tMOD	Max(24n CK,15ns)	-	Max(24n CK,15ns)	-	Max(24n CK,15ns)	-	Max(24n CK,15ns)	-	Max(24n CK,15ns)	-	Max(24n CK,15ns)	-	Max(24n CK,15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Re- covery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))															
DQ0 or DQ0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQ0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency																	
CS _n to Command Address La- tency	tCAL	Max(3 nCK, 3.748 ns)	-	Max(3 nCK, 3.748 ns)	-	Max(3 nCK, 3.748 ns)	-	Max(3 nCK, 3.748 ns)	-	Max(3 nCK, 3.748 ns)	-	Max(3 nCK, 3.748 ns)	-	Max(3 nCK, 3.748 ns)	-	nCK	
Mode Register Set command cy- cle time in CAL mode	tMRD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
DRAM Data Timing																	
DQS ₁ DQS _c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.17	-	0.18	-	0.19	-	0.20	tCK(avg)/2	13,18, 39,49

[Table 58] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-3200

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQ output hold time per group, per access from DQS _t , DQS _c	QH	0.76	-	0.76	-	0.76	-	0.74	-	0.74	-	0.72	-	0.70	-	tCK(avg)/2	13,17,18,39,49
Data Valid Window per device, per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	0.64	-	0.64	-	0.64	-	UI	17,18,39,49
Data Valid Window, per pin, per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	0.72	-	0.72	-	0.72	-	UI	17,18,39,49
DQ low impedance time from CK _t , CK _c	tLZ(DQ)	-450	225	-390	195	-360	180	-330	175	-310	170	-280	165	-250	160	ps	39
DQ high impedance time from CK _t , CK _c	tLZ(DQ)	-	225	-	195	-	180	-	175	-	170	-	165	-	160	ps	39
Data Strobe Timing																	
DQS _t , DQS _c differential READ Preamble (1 clock preamble)	tRPRE	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	tCK	40
DQS _t , DQS _c differential READ Preamble (2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	1.8	NOTE 44	1.8	NOTE 44	1.8	NOTE 44	1.8	NOTE 44	tCK	41
DQS _t , DQS _c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	
DQS _t , DQS _c differential output lowtime	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21
DQS _t , DQS _c differential WRITE Preamble (1 clock preamble)	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20
DQS _t , DQS _c differential WRITE Preamble (2 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS _t , DQS _c differential WRITE Postamble	tWPRE2	NA	-	NA	-	NA	-	NA	-	NA	-	NA	-	NA	-	tCK	43
DQS _t , DQS _c Differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS _t , DQS _c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-330	175	-310	170	-280	165	-250	160	ps	
DQS _t , DQS _c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	-	170	-	165	-	160	ps	
DQS _t , DQS _c Differentialinput low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS _t , DQS _c Differentialinput high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS _t , DQS _c rising edge to CK _t , CK _c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS _t , DQS _c rising edge to CK _t , CK _c rising edge (2 clock preamble)	tDQSS2	N/A	N/A	N/A	N/A	N/A	N/A	-0.5	0.5	-0.5	0.5	-0.5	0.5	-0.5	0.5	nCK	43
DQS _t , DQS _c falling edge setup time to CK _t , CK _c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	nCK	
DQS _t , DQS _c falling edge hold time to CK _t , CK _c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	nCK	
DQS _t , DQS _c rising edge output timing location from rising CK _t , CK _c rising edge with DLL On mode	tDQSK (DLL On)	-225	225	-195	195	-180	180	-175	175	-170	170	-165	165	-160	160	ps	37,38,39
DQS _t , DQS _c rising edge output variance window per DRAM	tDQSKV (DLL On)	-	370	-	330	-	310	-	290	-	270	-	265	-	260	ps	37,38,39
CS_n to Command Address Latency																	
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX (mi n)	-	tCKSRX (mi n)	-	tCKSRX (mi n)	-	tCKSRX (mi n)	-	tCKSRX (mi n)	-	tCKSRX (mi n)	-	tCKSRX (mi n)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-		
CS setup time to CKE	tMPX_S	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-		
CS _n High hold time to CKE rising edge	tMPX_HH	tXP(min)	-	tXP(min)	-	tXP(min)	-	tXP(min)	-	tXP(min)	-	tXP(min)	-	tXP(min)	-		

[Table 58] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-3200

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CS_n Low hold time to CKE rising edge	IMPX_LH	12	t _{IMP} ⁺ 10ns	12	t _{IMP} ⁺ 10ns	12	t _{IMP} ⁺ 10ns	12	t _{IMP} ⁺ 10ns	12	t _{IMP} ⁺ 10ns	12	t _{IMP} ⁺ 10ns	12	t _{IMP} ⁺ 10ns	ns	51
Calibration Timing																	
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	128	-	128	-	128	-	nCK	
Data Strobe Timing																	
Exit Reset from CKE HIGH to a valid command	tXPR	Max (5nCK, tRFC(min)+10ns)	-	Max (5nCK, tRFC(min)+10ns)	-	Max (5nCK, tRFC(min)+10ns)	-	Max (5nCK, tRFC(min)+10ns)	-	Max (5nCK, tRFC(min)+10ns)	-	Max (5nCK, tRFC(min)+10ns)	-	Max (5nCK, tRFC(min)+10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to ZOQL, ZQCS and MRS (CL, CWL, WR, RTP and Gear Down)	tXS_FAST(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDDL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKS-PE_PAR	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	Max (5nCK, 10ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	Max (5nCK, 10ns)	-	nCK	
Power Down Timing																	
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	Max (4nCK, 6ns)	-	nCK	
CKE minimum pulse width	tCKE	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	Max (3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK)(avg)	-	WL+4+(tWR/tCK)(avg)	-	WL+4+(tWR/tCK)(avg)	-	WL+4+(tWR/tCK)(avg)	-	WL+4+(tWR/tCK)(avg)	-	WL+4+(tWR/tCK)(avg)	-	WL+4+(tWR/tCK)(avg)	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK)(avg)	-	WL+2+(tWR/tCK)(avg)	-	WL+2+(tWR/tCK)(avg)	-	WL+2+(tWR/tCK)(avg)	-	WL+2+(tWR/tCK)(avg)	-	WL+2+(tWR/tCK)(avg)	-	WL+2+(tWR/tCK)(avg)	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	nCK	
PDA Timing																	
Mode Register Set command cycle time in PDA mode	tMRD_PDA	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	Max (16nCK, 10ns)	-	nCK	

[Table 58] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-3200

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		tMOD		tMOD		tMOD			
ODT Timing																	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic charge skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.28	0.72	0.26	0.74	0.26	0.74	tCK(avg)	
Write Leveling Timing																	
First DQS _t /DQS _c rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	40	-	40	-	40	-	nCK	12
DQS _t /DQS _c delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK _t , CK _c crossing to rising DQS _t /DQS _c crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising CK _t , CK _c crossing to rising DQS _t /DQS _c crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	0	2	0	2	0	2	ns	
CA Parity Timing																	
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	-	PL	-	PL	-	PL	tCK	
Delay from errant command to ALERT _n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	tCK	
Pulse width of ALERT _n signal when assertion	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	80	160	88	176	96	192	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	-	71	-	78	-	85	nCK	
Parity Latency	PL	4		4		4		5		5		6		6		nCK	
CRC Error Reporting																	
CRC error to ALERT _n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	3	13	3	13	3	13	ns	
CRC ALERT _n pulse width	tCRC_ALERT_PW	6	10	6	10	6	10	6	10	6	10	6	10	6	10	nCK	
Geardown Timing																	
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	-	-	-	-	-	-	-	-	tXPR	-	tXPR	-	tXPR	-		
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-	-	-	-	-	-	-	-	tXS	-	tXS	-	tXS	-		
MRS command to Sync pulse time(T3)	tSYN_C_GEAR	-	-	-	-	-	-	-	-	tMOD+4nCK	-	tMOD+4nCK	-	tMOD+4nCK	-		27
Sync pulse to First valid command(T4)	tCM_D_GEAR	-	-	-	-	-	-	-	-	tMOD	-	tMOD	-	tMOD	-		27
Geardown setup time	tGEAR_setup	-	-	-	-	-	-	-	-	2	-	2	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	-	-	-	-	-	-	2	-	2	-	2	-	nCK	
tREFI																	
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	350	-	350	-	350	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	260	-	260	-	260	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	160	-	160	-	160	-	ns	34

NOTE :

- 1) Start of internal write transaction is defined as follows :
 - For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
 - For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
 - For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
- 2) A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
- 3) Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
- 4) tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK following rounding algorithm defined in "15.1 Rounding Algorithms".
- 5) WR in clock cycles as programmed in MR0.
- 6) tREFI depends on TOPER.
- 7) CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
- 8) For these parameters, the DDR4 SDRAM device supports $t_{nPARAM}[nCK]=RU\{t_{PARAM}[ns]/t_{CK}(avg)[ns]\}$, which is in clock cycles assuming all input clock jitter specifications are satisfied.
- 9) When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
- 10) When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
- 11) When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
- 12) The max values are system dependent.
- 13) DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER.
- 14) The deterministic component of the total timing.
- 15) DQ to DQ static offset relative to strobe per group.
- 16) This parameter will be characterized and guaranteed by design.
- 17) When the device is operated with the input clock jitter, this parameter needs to be derated by the actual $t_{jit}(per)_{total}$ of the input clock. (output deratings are relative to the SDRAM input clock).
- 18) DRAM DBI mode is off.
- 19) DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
- 20) tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
- 21) tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
- 22) There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
- 23) tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
- 24) tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
- 25) Total jitter includes the sum of deterministic and random jitter terms for a specified BER.
- 26) The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
- 27) This parameter has to be even number of clocks
- 28) When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
- 29) When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
- 30) When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
- 31) After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
- 32) After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
- 33) Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
- 34) Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
- 35) This parameter must keep consistency with Speed-Bin Tables shown in section 10.
- 36) DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. $UI=tCK(avg).min/2$.
- 37) applied when DRAM is in DLL ON mode.
- 38) Assume no jitter on input clock signals to the DRAM.
- 39) Value is only valid for RONNOM = 34 ohms.
- 40) 1tCK toggle mode with setting MR4:A11 to 0.
- 41) 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/2933 and 3200 speed grade.
- 42) 1tCK mode with setting MR4:A12 to 0.
- 43) 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/2933 and 3200 speed grade.
- 44) The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Figure "Clock to Data Strobe Relationship" in Operation datasheet. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in "Read Preamble" section.
- 45) DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
- 46) last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
- 47) VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
- 48) The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Figure "Clock to Data Strobe Relationship" in Operation datasheet.
- 49) Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately $0.7 * VDDQ$ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to $VTT = VDDQ$.
- 50) For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.
- 51) tMPX_LH(max) is defined with respect to actual tXMP in system as opposed to tXMP(min).

15.1 Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as tCKAVGmin are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.
- Using real math, parameters like tAmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:

$$nCK = \text{ceiling} [(parameter_in_ns / application_tCK_in_ns) - 0.025]$$

- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:

$$nCK = \text{truncate} [\{ (parameter_in_ps \times 1000) / (application_tCK_in_ps) + 974 \} / 1000]$$

- Either algorithm yields identical results. In case of conflict between results, the preferred algorithm is the integer math algorithm.
- This algorithm applies to all timing parameters documented in a Serial Presence Detect (SPD) when converting from ns to nCK. Other timing parameters may use a simpler algorithm

$$nCK = \text{ceiling} (parameter_in_ns / application_tCK_in_ns)$$

15.2 The DQ input receiver compliance mask for voltage and timing

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal with BER of 1e-16; any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye.

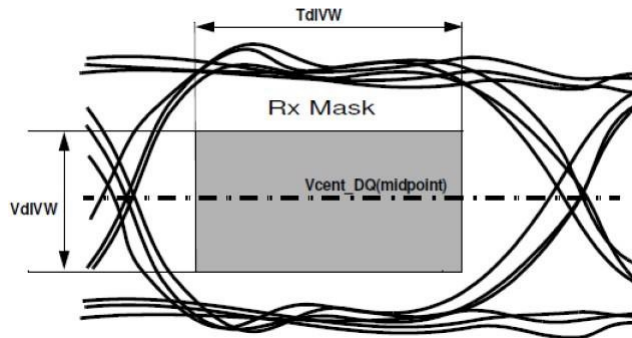


Figure 24. DQ Receiver(Rx) compliance mask

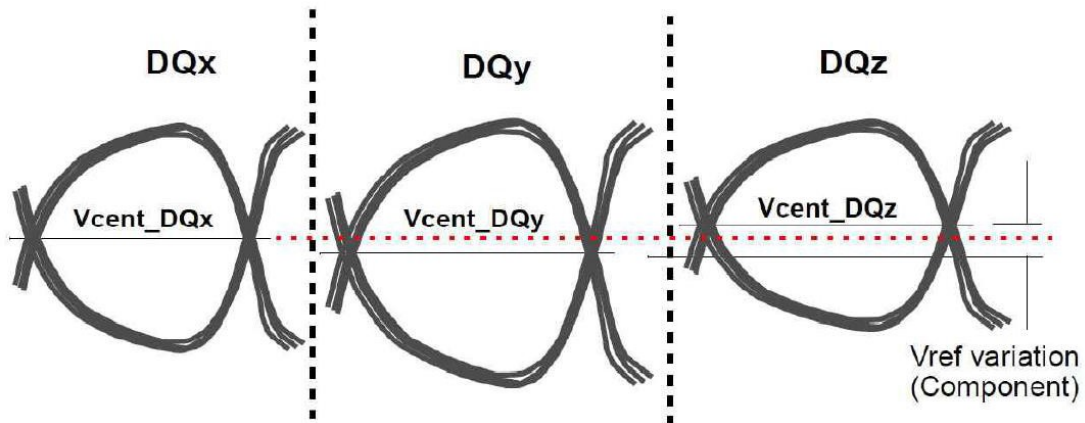
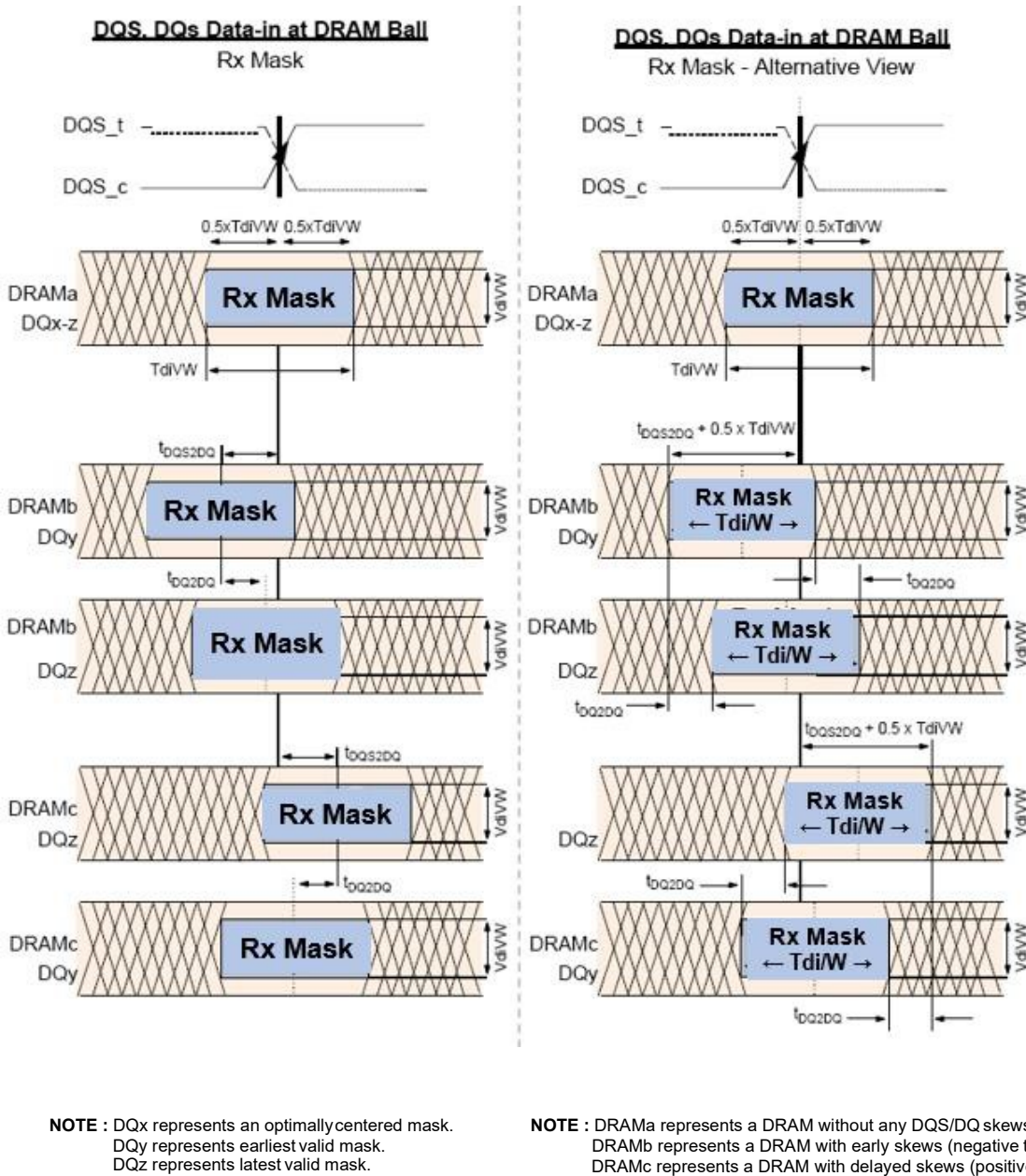


Figure 25. Vcent_DQ Variation to Vcent_DQ(midpoint)

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values.

Vcent_DQ is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 25. This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask. The component level Vref will be set by the system to account for Ron and ODT settings.



NOTE : Figures show skew allowed between DRAM to DRAM and DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch.
 t_{DiPW} is not shown; composite data-eyes shown would violate t_{DiPW} .
Vcent DQ(midpoint) is not shown but is assumed to be midpoint of V_{diVW} .

Figure 26. DQS to DQ and DQ to DQ Timings at DRAM Balls

All of the timing terms in Figure 26 are measured at the V_{diVW} voltage levels centered around V_{cent_DQ} and are referenced to the DQS_t/DQS_c center aligned to the DQ per pin.

The rising edge slew rates are defined by $srr1$ and $srr2$. The slew rate measurement points for a rising edge are shown in Figure 27 below: A low to high transition $tr1$ is measured from $0.5 \cdot V_{diVW}(\max)$ below $V_{cent_DQ}(\text{midpoint})$ to the last transition through $0.5 \cdot V_{diVW}(\max)$ above $V_{cent_DQ}(\text{midpoint})$

while $tr2$ is measured from the last transition through $0.5 \cdot V_{diVW}(\max)$ above $V_{cent_DQ}(\text{midpoint})$ to the first transition through the $0.5 \cdot V_{IHL_AC}(\min)$ above $V_{cent_DQ}(\text{midpoint})$.

Rising edge slew rate equations:

$$srr1 = VdiVW(max) / tr1$$

$$srr2 = (VIHL_AC(min) - VdiVW(max)) / (2*tr2)$$

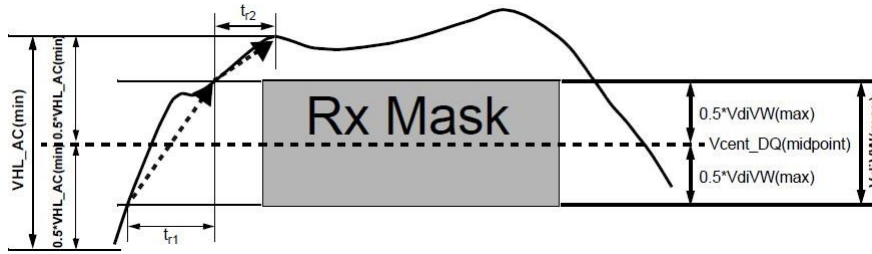


Figure 27. Slew Rate Conditions For Rising Transition

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in Figure 28 below: A high to low transition tf1 is measured from 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) while tf2 is measured from the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) below Vcent_DQ(pin mid).

Falling edge slew rate equations:

$$srf1 = VdiVW(max) / tf1$$

$$srf2 = (VIHL_AC(min) - VdiVW(max)) / (2*tf2)$$

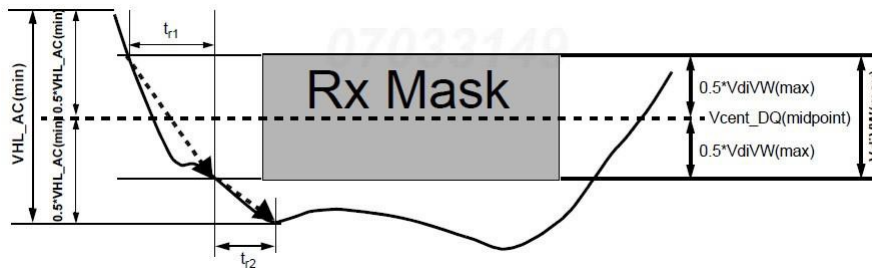


Figure 28. Slew Rate Conditions For Falling Transition

[Table 59] DRAM DQs In Receive Mode;

Symbol	Parameter	1600/1866/2133		2400		2666		2933		3200		Unit	Note
		min	max	min	max	min	max	min	max	min	max		
VdIVW	Rx Mask voltage - pk-pk	-	136	-	130	-	120	-	115	-	110	mV	1,2,10
TdIVW	Rx timing window	-	0.2	-	0.2	-	0.22	-	0.23	-	0.23	UI*	1,2,10
VIHL_AC	DQ AC input swing pk-pk	186	-	160	-	150	-	145	-	140	-	mV	3,4,10
TdIPW	DQ input pulse width	0.58	-	0.58	-	0.58	-	0.58	-	0.58	-	UI*	5,10
tDQS2DQ	Rx Mask DQS to DQ offset	-0.17	0.17	-0.17	0.17	-0.19	0.19	-0.22	0.22	-0.22	0.22	UI*	6, 10
tDQ2DQ	Rx Mask DQ to DQ offset	-	0.1	-	0.1	-	0.105	-	0.115	-	0.125	UI*	7
srr1, srf1	Input Slew Rate over VdIVW if tCK >= 0.937ns	1.0	9	1.0	9	1.0	9	1.0	9	1.0	9	V/ns	8,10
	Input Slew Rate over VdIVW if 0.937ns > tCK >= 0.625ns	-	-	1.25	9	1.25	9	1.25	9	1.25	9	V/ns	8,10
srr2	Rising Input Slew Rate over 1/2 VIHL_AC	0.2*srr 1	9	0.2*srr 1	9	0.2*srr 1	9	0.2*srr 1	9	0.2*srr 1	9	V/ns	9,10
srf2	Falling Input Slew Rate over 1/2 VIHL_AC	0.2*srf 1	9	0.2*srf 1	9	0.2*srf 1	9	0.2*srf 1	9	0.2*srf 1	9	V/ns	9,10

* UI=tck(avg)min/2

NOTE :

- 1) Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER = e-16 when the RxMask is not violated.
- 2) Defined over the DQ internal Vref range 1.
- 3) See Overshoot and Undershoot Specifications.
- 4) DQ input pulse signal swing into the receiver must meet or exceed VIHL_AC(min). VIHL_AC(min) is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e. a valid TdIPW.
- 5) DQ minimum input pulse width defined at the Vcent_DQ(midpoint).
- 6) DQS to DQ offset is skew between DQS and DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls over process, voltage, and temperature.
- 7) DQ to DQ offset is skew between DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.
- 8) Input slew rate over VdIVW Mask centered at Vcent_DQ(midpoint). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7 V/ns of each other.
- 9) Input slew rate between VdIVW Mask edge and VIHL_AC(min) points.
- 10) All Rx Mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdIVW(min), VdIVW(max), and minimum slew rate limits, then either TdIVW(min) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

15.3 Command, Control, and Address Setup, Hold, and Derating

The total tIS (setup time) and tIH (hold time) required is calculated to account for slew rate variation by adding the data sheet tIS (base) values, the VIL(AC)/VIH(AC) points, and tIH (base) values, the VIL(DC)/VIH(DC) points; to the ΔtIS and ΔtIH derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example: tIS (total setup time) = tIS (base) + ΔtIS.

For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for the time defined by tVAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/ VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/ VIL(AC). For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)max that does not ring back above VIL(DC)max. Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)min that does not ring back above VIL(DC)max.

[Table 60] Command, Address, Control Setup and Hold Values

DDR4	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
tIS(base, AC100)	115	100	80	62	-	-	-	ps	VIH/L(ac)
tIH(base, DC75)	140	125	105	87	-	-	-	ps	VIH/L(dc)
tIS(base, AC 90)	-	-	-	-	55	48	40	ps	VIH/L(ac)
tIH(base, DC 65)	-	-	-	-	80	73	65	ps	VIH/L(dc)
tIS/tIH @ VREF	215	200	180	162	145	138	130	ps	

NOTE :

- 1) Base ac/dc referenced for 1V/ns slew rate and 2 V/ns clock slew rate.
- 2) Values listed are referenced only; applicable limits are defined elsewhere

[Table 61] Command, Address, Control Input Voltage Values

DDR4	1600	1866	2133	2400	2666	2933	3200	Unit	Reference
VIH.CA(AC)min	100	100	100	100	90	90	90	mV	VIH/L(ac)
VIH.CA(DC)min	75	75	75	75	65	65	65	mV	VIH/L(dc)
VIL.CA(DC)min	-75	-75	-75	-75	-65	-65	-65	mV	VIH/L(dc)
VIL.CA(AC)min	-100	-100	-100	-100	-90	-90	-90	mV	VIH/L(ac)

NOTE :

- 1) Command, Address, Control input levels relative to VREFCA.
- 2) Values listed are referenced only; applicable limits are defined elsewhere

[Table 62] Derating values DDR4-1600/1866/2133/2400 tIS/tIH - ac/dc based

ΔtIS, ΔtIH derating in [ps] AC/DC based ¹⁾																	
		CK_t, CK_c Differential Slew Rate															
		10V/ns		8V/ns		6V/ns		4V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD, ADDR, CNTL Input Slew rate V/ns	7	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
	6	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
	5	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
	4	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
	3	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
	2	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
	1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
	1	-10	-10	-9	-9	-8	-8	-6	-6	-4	-4	0	0	8	8	25	25
	0.9	-17	-14	-16	-14	-15	-13	-13	-10	-11	-8	-7	-4	1	4	18	21
	0.8	-26	-19	-25	-19	-24	-18	-22	-16	-20	-14	-16	-9	-7	-1	9	16
	0.7	-37	-26	-36	-25	-35	-24	-33	-22	-31	-20	-27	-16	-18	-8	-2	9
	0.6	-52	-35	-51	-34	-50	-33	-48	-31	-46	-29	-42	-25	-33	-17	-17	0
	0.5	-73	-48	-72	-47	-71	-46	-69	-44	-67	-42	-63	-38	-54	-29	-38	-13
0.4	-104	-66	-103	-66	-102	-65	-100	-63	-98	-60	-94	-56	-85	-48	-69	-31	

NOTE :

1) VIH/L(ac) = +/-100mV, VIH/L(dc) = +/-75mV: relative to VREFCA.

[Table 63] Derating values DDR4-2666/2933/3200 tIS/tIH - ac/dc based

ΔtIS, ΔtIH derating in [ps] AC/DC based ¹⁾																	
		CK_t, CK_c Differential Slew Rate															
		10V/ns		8V/ns		6V/ns		4V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD, ADDR, CNTL Input Slew rate V/ns	7	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	6	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	5	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	4	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	3	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	2	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	1	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	0	0	8	8	23	23
	0.9	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	0.8	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	0.7	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
	0.6	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	0.5	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
0.4	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26	

NOTE :

1) VIH/L(ac) = +/-90mV, VIH/L(dc) = +/-65mV: relative to VREFCA

15.4 DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

[Table 64] Function Matrix (By ORG. V: Supported, Blank: Not supported)

Functions	x16	Note
Write Leveling	V	
Temperature controlled Refresh	V	
Low Power Auto Self Refresh	V	
Fine Granularity Refresh	V	
Multi Purpose Register	V	
Data Mask	V	
Data Bus Inversion	V	
TDQS		
ZQ calibration	V	
DQ Vref Training	V	
Per DRAM Addressability	V	
Mode Register Readout	V	
CAL	V	
WRITE CRC	V	
CA Parity	V	
Control Gear Down Mode	V	
Programmable Preamble	V	
Maximum Power Down Mode		
Boundary Scan Mode	V	
Additive Latency		

[Table 65] Function Matrix (By Speed. V:Supported, Blank:Not supported)

Functions	DLL Off mode	DLL On mode			Note
	equal or slower than 250Mbps	1600/1866/2133Mbps	2400Mbps	2666/2933/3200Mbps	
Write Leveling	V	V	V	V	
Temperature controlled Refresh	V	V	V	V	
Low Power Auto Self Refresh	V	V	V	V	
Fine Granularity Refresh	V	V	V	V	
Multi Purpose Register	V	V	V	V	
Data Mask	V	V	V	V	
Data Bus Inversion	V	V	V	V	
TDQS		V	V	V	
ZQ calibration	V	V	V	V	
DQ Vref Training	V	V	V	V	
Per DRAM Addressability		V	V	V	
Mode Register Readout	V	V	V	V	
CAL		V	V	V	
WRITE CRC		V	V	V	
CA Parity		V	V	V	
Control Gear Down Mode				V	
Programmable Preamble (= 2tCK)			V	V	
Maximum Power Down Mode		V	V	V	
Boundary Scan Mode	V	V	V	V	