Cover Sheet and Revision Status				
版別 (Rev.)	DCC No.	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	-	Aug. 17, 2016	New issue	Hank Lin
2.0	20200019	Dec. 29, 2020	Revise ICC (operating current) 45ns- 30mA, 55ns- 30mA, 70ns- 25mA	Hank Lin

PRODUCT DESCRIPTION

The CS18LV82933 is a high performance, high speed, low power CMOS Static Random Access Memory organized as 1M words by 8 bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced 90nm Full CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.3uA and maximum access time of 45/55/70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable1 (/CE1), active HIGH chip enable2 (CE2) and active LOW output enable (/OE) and three-state output drivers.
The CS18LV82933 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS18LV82933 is available in Jedec standard 44L TSOP 2 and 48TFBGA-6x8mm packages.

FEATURES

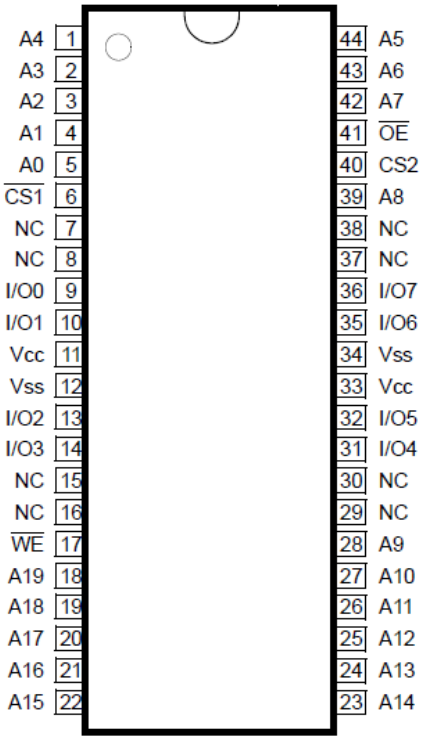
- Low operation voltage: 2.7 ~ 3.6V
- Ultra low power consumption :
  - operating current: 30mA (Max.) @t_{AA}=45ns
- Fast access time: 45/55/70ns (Max.)
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible, fully static operation
- Data retention supply voltage as low as 1.5V.

PRODUCT FAMILY

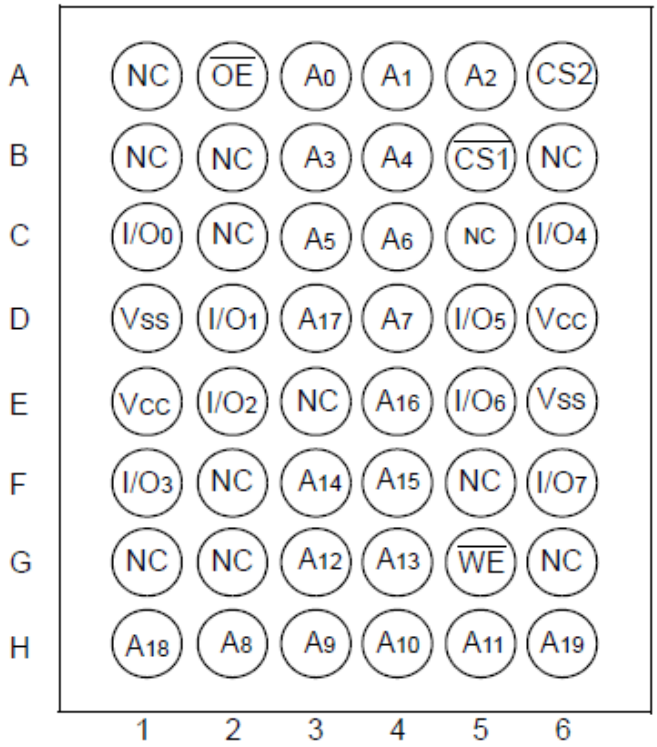
Product Family	Operating Temp	V_{CC}. Range (V)	Speed (ns)	Package Type
CS18LV82933	0 ~ 70°C	2.7 ~ 3.6	45/55/70	44 TSOP 2 48 TFBGA
	-40 ~ 85°C			

PIN CONFIGURATIONS

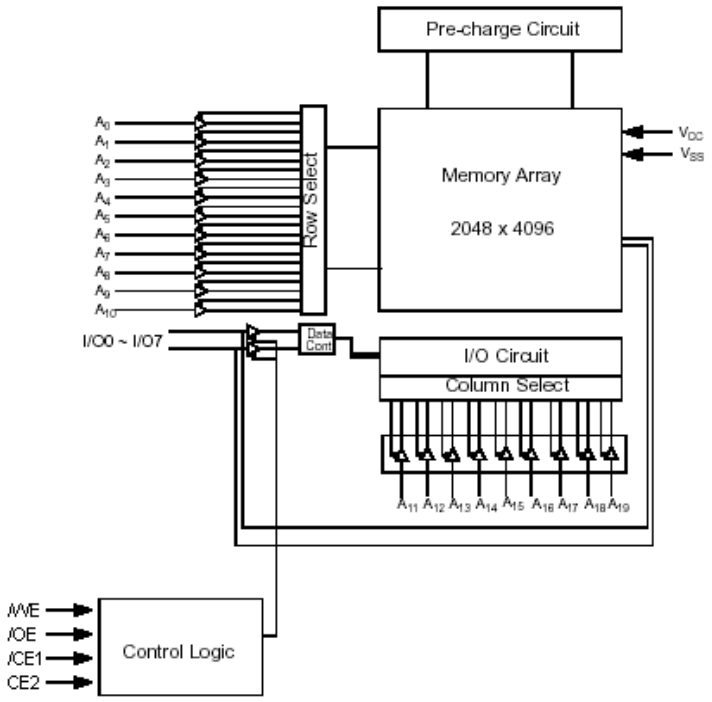
44 TSOP2



48 TFBGA



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Type	Function
A0 – A19	Input	20 address inputs for selecting one of the 1M x 8 bit words in the RAM
/CE1 & CE2	Input	/CE1 is active LOW and CE2 is active high. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and in a standby power mode. The I/O pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the I/O pins, when /WE is LOW, the data present on the I/O pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the I/O pins and they will be enabled. The I/O pins will be in the high impedance state when /OE is inactive.
I/O0~I/O7	I/O	These 8 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power	Power Supply
V_{SS}	Power	Ground

TRUTH TABLE

MODE	/CE1	CE2	/WE	/OE	I/O0~I/O7	V_{CC} Current
Standby	H	X	X	X	High Z	I_{CCSB}, I_{CCSB1}
	X	L	X	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	H	High Z	I_{CC}
Read	L	H	H	L	D_{OUT}	I_{CC}
Write	L	H	L	X	D_{IN}	I_{CC}

Note: X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit
V_{IN} , V_{OUT}	Voltage on Any Pin Relative to V_{SS}	-0.5 to Vcc+0.5V	V
V_{CC}	Voltage on V_{CC} supply Relative to V_{SS}	-0.5 to 4.6	V
T_A	Operating Temperature	-40 to +85	^{O}C
P_D	Power Dissipation	1.0	W

1. *Stresses greater than those listed above "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

OPERATING RANGE

Range	Ambient Temperature	V_{CC}
Commercial	0~70°C	2.7V ~ 3.6V
Industrial	-40~85°C	2.7V ~ 3.6V

DC ELECTRICAL CHARACTERISTICS (TA = 0~70℃ / -40℃~85℃, VCC = 3.0V)

Parameter Name	Parameter	Test Conduction	MIN	TYP	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage (2)		-0.3		0.8	V
V_{IH}	Guaranteed Input High Voltage (1)		2.2		Vcc+0.3	V
I_{IL}	Input Leakage Current	V_{IN}=V_{SS} to V_{CC}	-1		1	uA
I_{OL}	Output Leakage Current	/CE1=V_{IH} and CE2=V_{IL}, or /OE=V_{IH} or /WE=V_{IL} or V_{IO}=V_{SS} to V_{CC}	-1		1	uA
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1mA	2.4			V

I_{CC}	Operating Power Supply Current	/CE1=V_{IL} and CE2=V_{IH}, I_{IO}=0mA, F=F_{MAX}(2)	45ns			25	mA
			55ns			25	
			70ns			20	
I_{CCSB}	Standby Supply - TTL	/CE1=V_{IH} and CE2=V_{IL}, Other pins= V_{IH} or V_{IL}				0.5	mA
I_{CCSB1}	Standby Current-CMOS	/CE1≧V_{CC}-0.2V or CE2≦0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V				15	uA

1. *Overshoot: Vcc+2.0V in case of pulse width≤20ns,*

   Undershoot:-2.0V in case of pulse width≤20ns

   Overshoot and undershoot are sampled, not 100% tested.

2. *Fmax = 1/t_{RC}.*

CAPACITANCE (1) (TA = 25℃, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{IO}	Input/output Capacitance	$V_{I/O}$=0V	8	pF

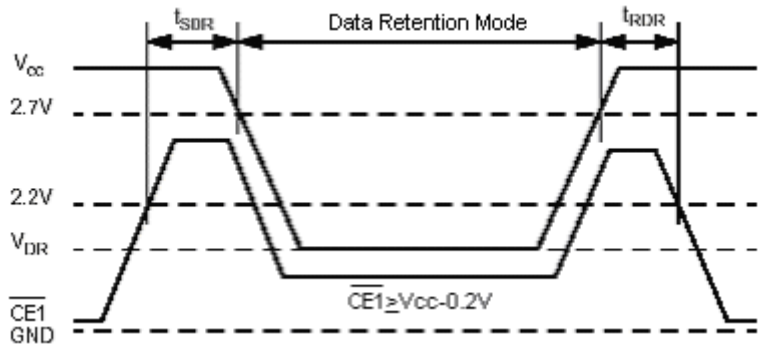
1. *Capacitance is samples, not 100% tested.*

DATA RETENTION CHARACTERISTICS (TA = 0~+70℃ / -40℃~+85℃)

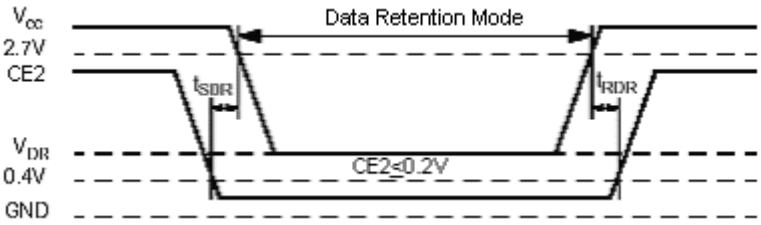
Parameter Name	Parameter	Test Conduction	MIN	TYP	MAX	Unit
V_{DR}	V_{CC} for Data Retention	/CE1≧V_{CC}-0.2V or CE2≦0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	1.5			V
I_{CCDR}	Data Retention Current	/CE1≧V_{CC}-0.2V or CE2≦0.2V, V_{CC}=1.5V V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V			15	uA
t_{SDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0			ns
t_{RDR}	Operation Recovery Time		t_{RC}(1)			ns

1. *t_{RC}= Read Cycle Time.*

LOW V_{CC} DATA RETENTION WAVEFORM (1) (/CE1 Controlled)



LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)



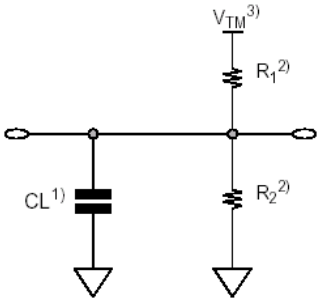
AC TEST CONDITIONS

Input Pulse Levels	0V~2.5V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Level	1.5V
Output Load	See Below

KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
———	MUST BE STEADY	MUST BE STEADY
⟋⟋⟋	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L

AC TEST LOADS



1. Including scope and Jig capacitance
2. R_1=3070 ohm, R_2=3150 ohm
3. V_{TM}=2.8V

	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

AC ELECTRICAL CHARACTERISTICS (TA = 0~+70℃ / -40℃~+85℃, VCC = 3.0V)

< READ CYCLE >

JEDEC Parameter Name	Parameter Name	Description	45ns		55ns		70ns		Unit
			Min	Max	Min	Max	Min	Max	
t_{AVAX}	t_{RC}	Read Cycle Time	45		55		70		ns
t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns
t_{ELQV}	t_{CO}	Chip Select Access Time (/CE1, CE2)		45		55		70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		22		25		35	ns
t_{ELQX}	t_{LZ}	Chip Select to Output Low Z (/CE1, CE2)	10		10		10		ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		5		5		ns
t_{EHQZ}	t_{HZ}	Chip Deselect to Output in High Z (/CE1, CE2)		18		20		25	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		18		20		25	ns
t_{AXOX}	t_{OH}	Out Disable to Address Change	10		10		10		ns

AC ELECTRICAL CHARACTERISTICS (TA = 0~+70℃ / -40℃~+85℃, VCC = 3.0V)

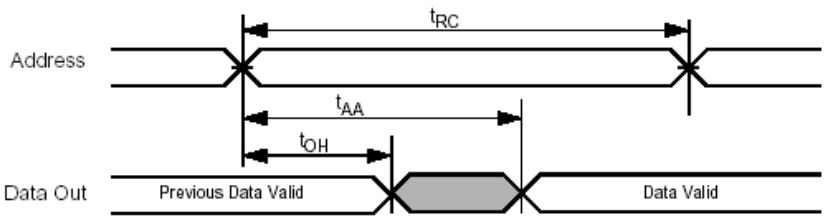
< WRITE CYCLE >

JEDEC Parameter Name	Parameter Name	Description	45ns		55ns		70ns		Unit
			Min	Max	Min	Max	Min	Max	
t_{AVAX}	t_{WC}	Write Cycle Time	45		55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	35		40		60		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	35		45		60		ns
t_{WLWH}	t_{WP}	Write Pulse Width	35		40		55		ns
t_{WHAX}	t_{WR}	Write Recovery Time (/CE1, CE2, /WE)	0		0		0		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		18		20		25	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25		25		30		ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0		0		0		ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5		5		5		ns

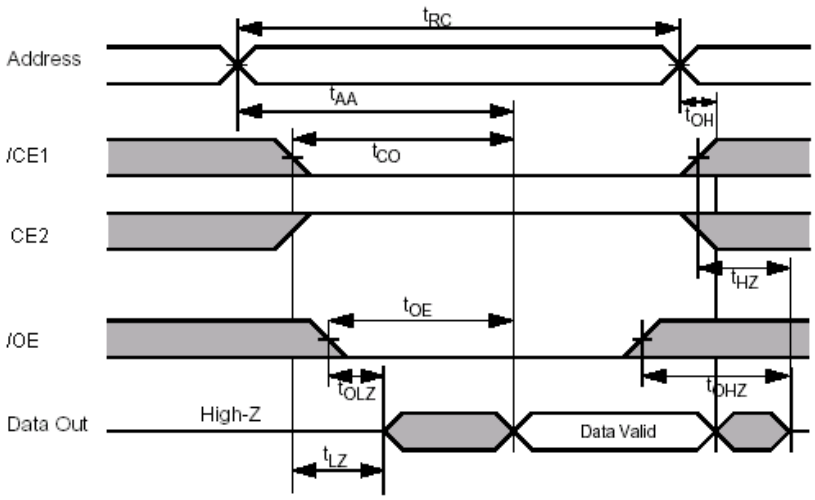
SWITCHING WAVEFORMS (READ CYCLE)

Read CYCLE 1.

(Address Controlled, /CE1=/OE=VIL, CE2=/WE=VIH)



Read CYCLE 2. (/WE=VIH)

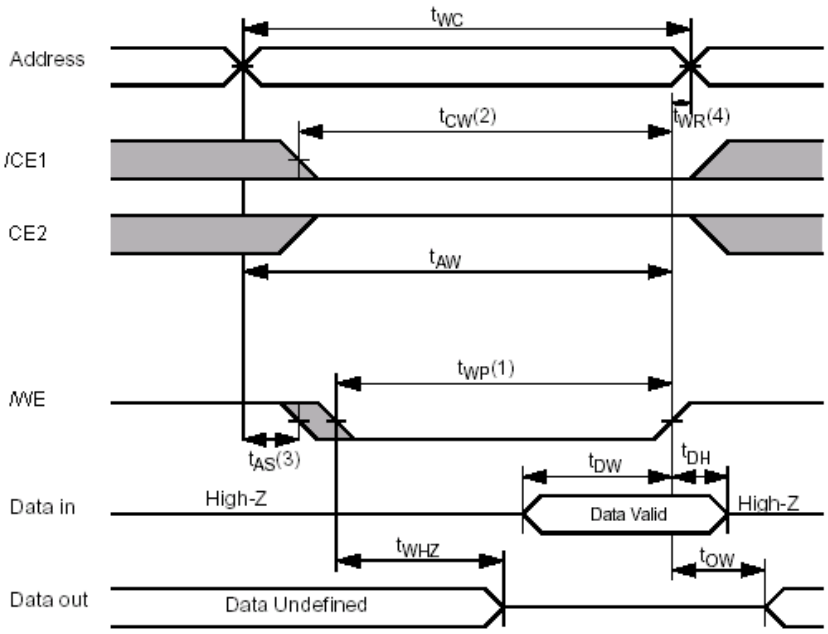


NOTES:

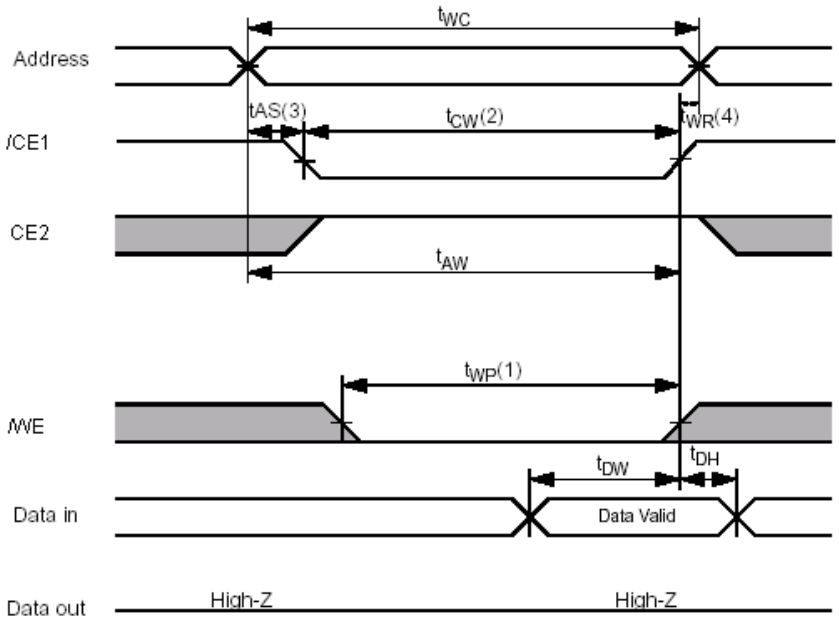
1. *t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
2. *At any given temperature and voltage condition, t_{HZ} (Max.) is less than t_{LZ} (Min.) both for a given device and from device to device interconnection.*

SWITCHING WAVEFORMS (WRITE CYCLE)

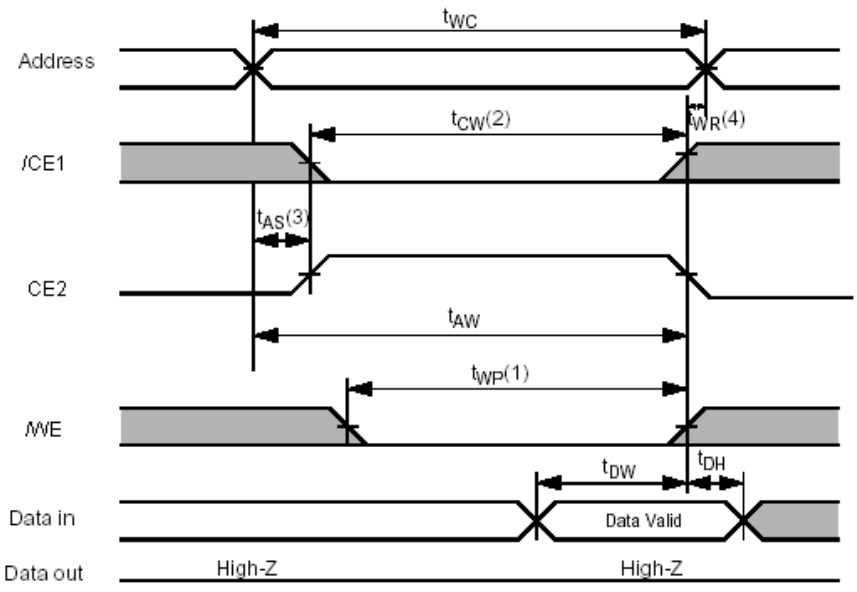
WRITE CYCLE 1 (/WE Controlled)



WRITE CYCLE 2 (/CE1 Controlled)



WRITE CYCLE 3 (CE2 Controlled)

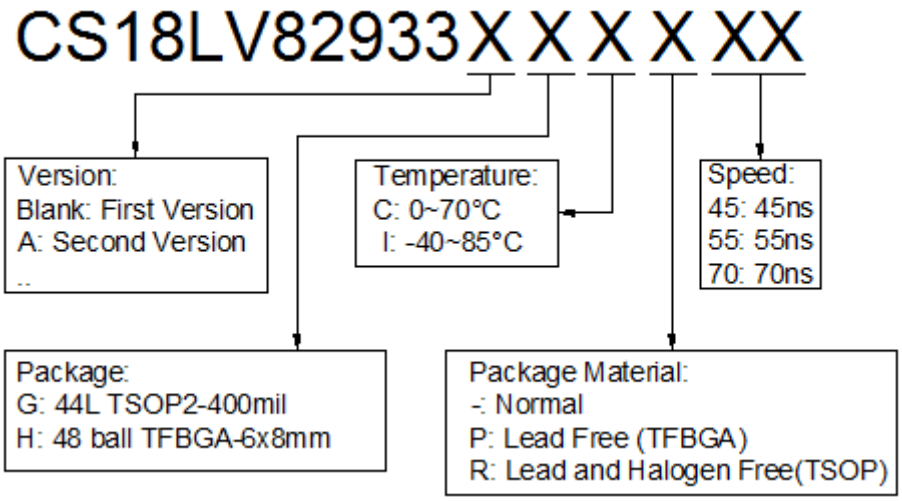


NOTES:

1. *A write occurs during the overlap (t_{WP}) of low /CE1, high CE2 and low /WE. A write begins when /CE1 goes low, CE2 goes high and /WE goes low. A write ends at the earliest transition when /CE1 goes high, CE2 goes low and /WE goes high. The t_{WP} is measured from the beginning of the write to the end of write.*
2. *t_{CW} is measured from the /CE1 going low or CE2 going low to end of write.*
3. *t_{AS} is measured from the address valid to the beginning of write.*
4. *t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as /CE1 or /WE going high or CE2*

going low.

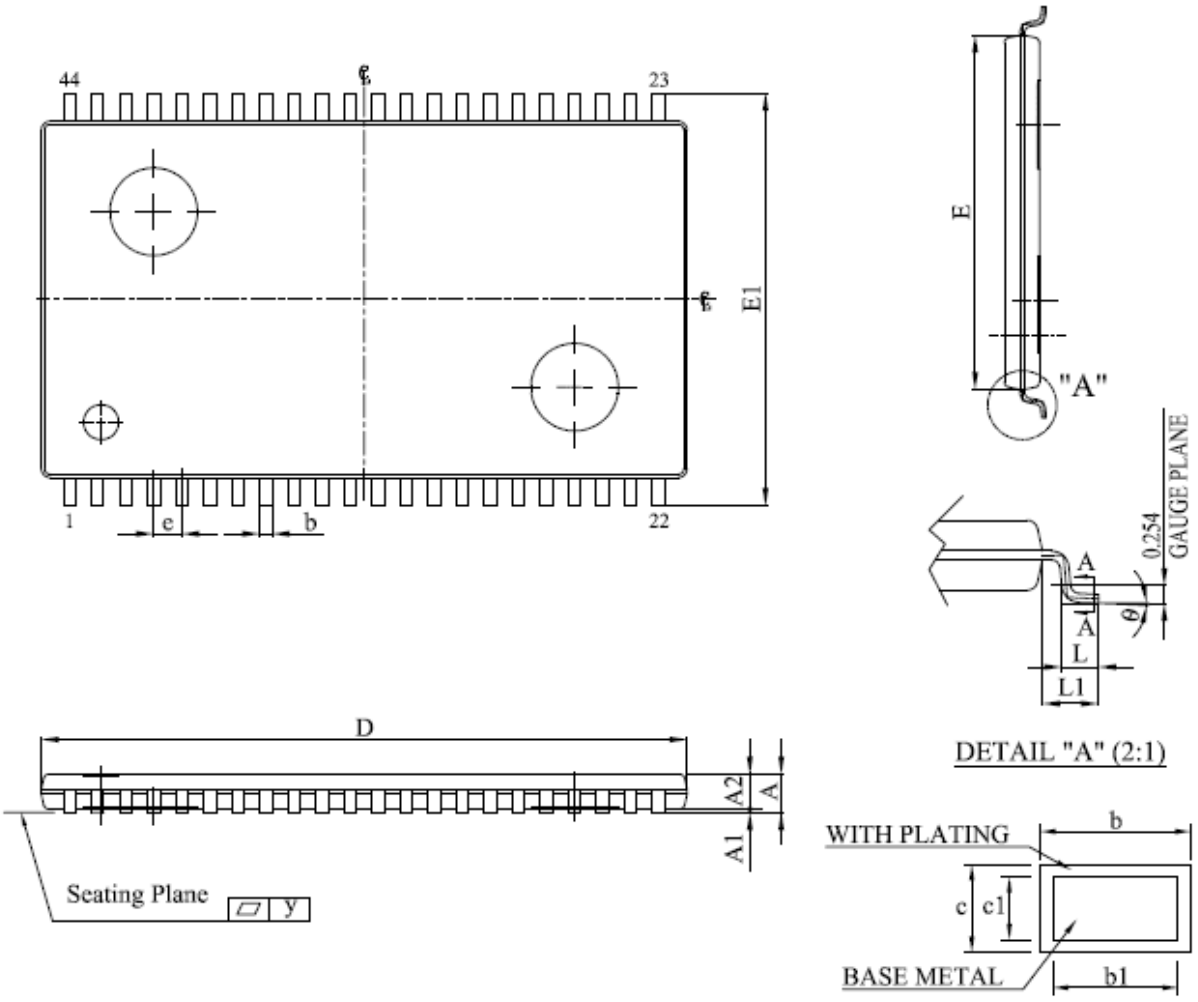
ORDER INFORMATION



Note: Package material code "R" meet RoHS.

PACKAGE OUTLINE

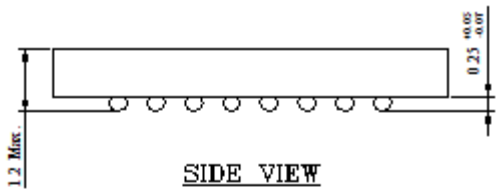
44L TSOP2-400mil



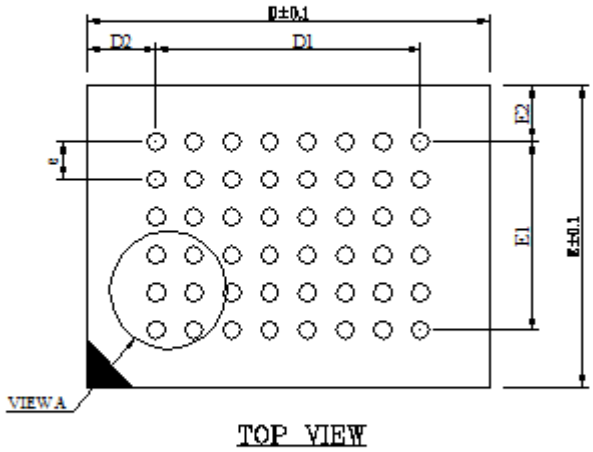
Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

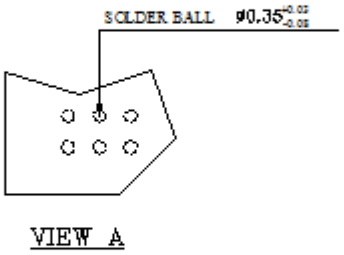
SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	Θ
mm	Min.	1.00	0.05	0.95	0.30	0.30	0.12	0.12	18.31	10.06	11.56	0.70	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	–	–	–	–	18.41	10.16	11.76	0.80	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.45	0.40	0.21	0.16	18.51	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.012	0.012	0.005	0.005	0.721	0.396	0.455	0.0275	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	–	–	–	–	0.725	0.400	0.463	0.0315	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.018	0.016	0.008	0.006	0.729	0.404	0.471	0.0355	0.0237	0.0355	0.004	8°

48 ball TFBGA-6x8mm



BALL PITCH e=0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125





NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
   LINEAR : X.X = ±0.1
   X.XX = ±0.05
   X.XXX = ±0.025