Cover Sheet and Revision Status				
版別 (Rev.)	DCC No	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20210013	12-Apr.-2021	New issue	Hank Lin
2.0	20210026	06-Aug-2021	Delete deep power down mode function	Hank Lin

Product Description

The CS26LV16183 is a high performance, high speed, low power pseudo SRAM organized as 1M words by 16 bits and operates from a wide range of 2.6 to 3.6V supply voltage. Advanced DRAM technology and circuit techniques provide both high speed and maximum access time of 70ns in 3.3V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE) and three-state output drivers. The CS26LV16183 is available 48-ball TFBGA package.

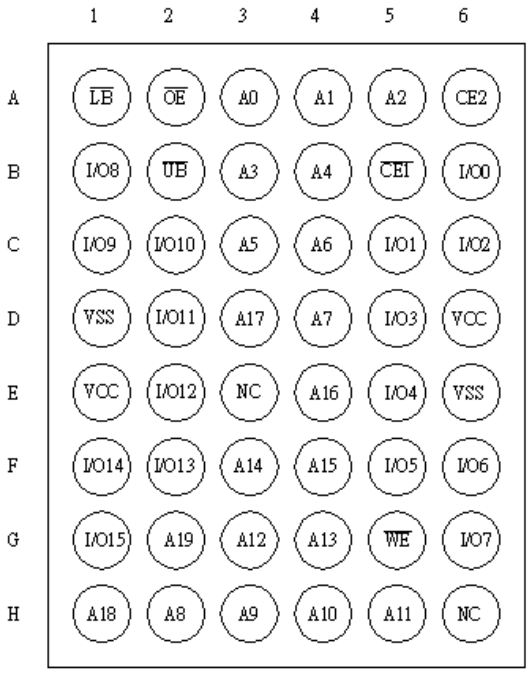
Features

- Single power supply voltage of 2.6 to 3.6V
- Direct TTL compatibility for all inputs and outputs.
- Page read operation by 8 words.
- Logic compatible with SRAM R/W pin.
- Standby Current
  - Standby 100 uA (Max.)
- Access Time
  - /CE1 Access Time: 70ns
  - /OE Access Time: 45ns
  - Page Access Time: 25ns

Product Family

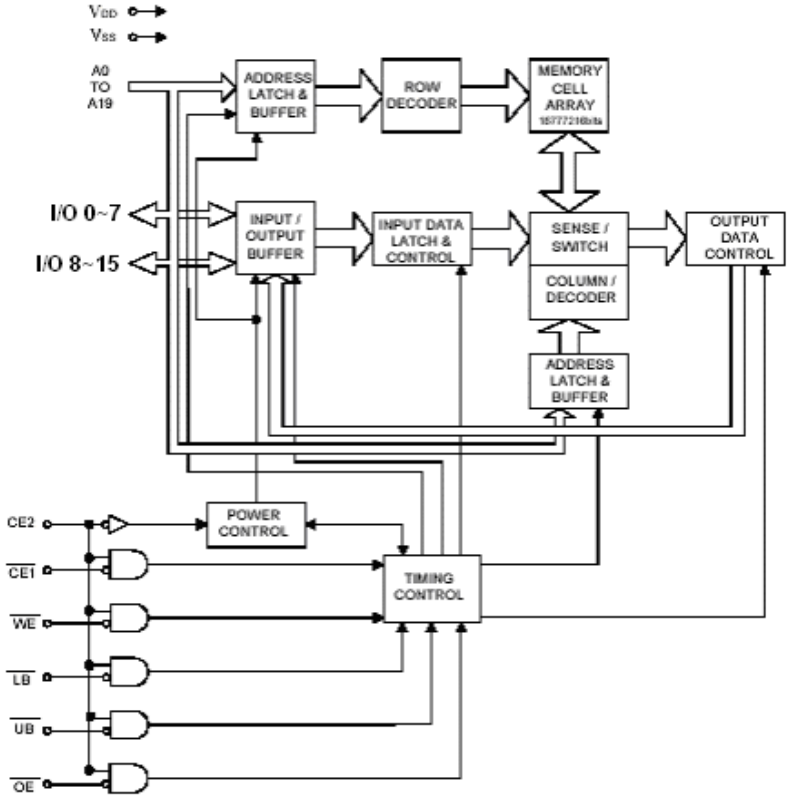
Part No.	Operating Temp	Vcc. Range	Speed	Standby (ISB, Max.)	Package Type
CS26LV16183	0~70 °C	2.6~3.6V	70ns	120uA	Dice
	-40~85 °C				48 TFBGA-6x8mm

Pin Configuration



48 Ball TFBGA Top View

Functional Block Diagram



Pin Description

Name	Type	Function
A0~A19	input	Address inputs
/CE1	input	Chip enables input 1. Low: enable
CE2	input	Chip enable input 2. High: enable, Low: enter power down mode
/WE	input	Write enable input
/OE	input	Output enable input
/LB	input	Lower byte data input/output control pin
/UB	input	Upper byte data input/output control pin
I/O0~I/O15	I/O	Data input/output pins
V_{CC}	Power	Power Supply
V_{SS}	Power	Ground
NC		No connection

Truth Table

MODE	/CE1	CE2	/OE	/WE	/LB	/UB	DQ0~7	DQ8~15	V_{DD} Current
Standby	H	H	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	L	H	L	L	D_{OUT}	D_{OUT}	I_{CC}
Upper Byte Read					L	H	D_{OUT}	High Z	I_{CC}
Lower Byte Read					H	L	High Z	D_{OUT}	I_{CC}
Write	L	H	X	L	L	L	D_{IN}	D_{IN}	I_{CC}
Upper Byte Write					L	H	D_{IN}	Invalid	I_{CC}
Lower Byte Write					H	L	Invalid	D_{IN}	I_{CC}

Note: X means don't care. (Must be low or high state)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Voltage of V_{CC} supply relative to V_{SS}	-0.2 to 3.6	V
V_{IN} , V_{OUT}	Voltage at any pin relative to V_{SS}	-0.2 to Vcc+0.3	V
T_{STG}	Storage Temperature	-65 to +125	^{O}C
P_T	Power Dissipation	1.0	W

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (TA = 0 to + 70°C , V_{CC} = 2.6V to 3.6V)

Parameter Name	Parameter	Test Conduction	MIN	TYP	MAX	Unit
V_{IL}	Input Low Voltage (1)		-0.2		0.6	V
V_{IH}	Input High Voltage (1)		2.2		Vcc+0.2	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}	-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE1=V_{IN}, or /OE=V_{IN} , V_{IO}=0V to V_{CC}	-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} = 2mA			0.2*Vcc	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -1mA	0.8*Vcc			V
I_{CC1}	Operating Power Supply Current	Cycle time=Min, I_{IO}=0mA, 100% duty, /CE1=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IL} or V_{IH}			35	mA
I_{SB1}	Standby Current - CMOS	/CE1 & CE2≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V			100	uA

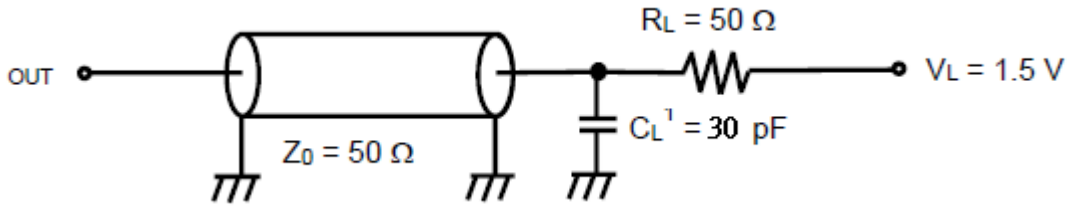
1. V_{IH}(Max) V_{CC}+1.0V with 10ns pulse width, V_{IL}(Min)-1.0V with 10ns pulse width

Capacitance (1) (TA = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{DQ}	Input /Output Capacitance	$V_{I/O}$=0V	10	pF

This parameter is guaranteed and not tested.

AC Test Conditions



Including scope and jig capacitance

Standby Mode Characteristics

Power Mode	Memory Cell Data	Standby Current (uA)	Write Time
Standby	Valid	100	0

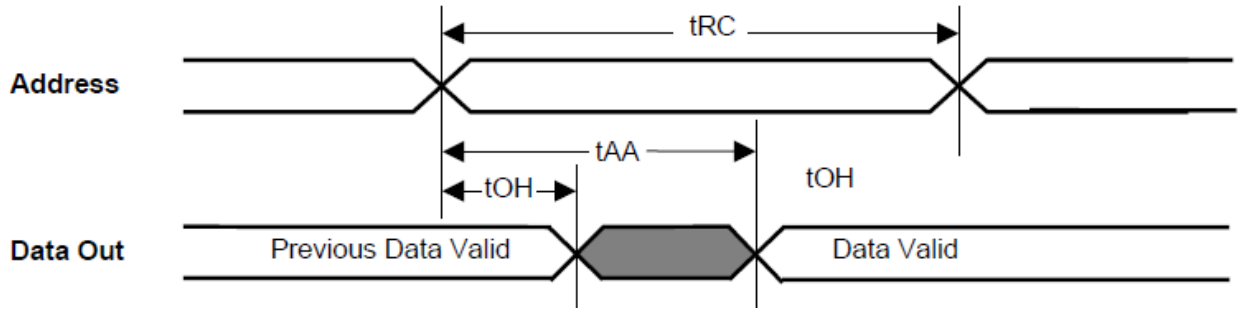
AC Characteristics (T_A = 0 to + 70°C, V_{CC}= 3.3V)

Read cycle

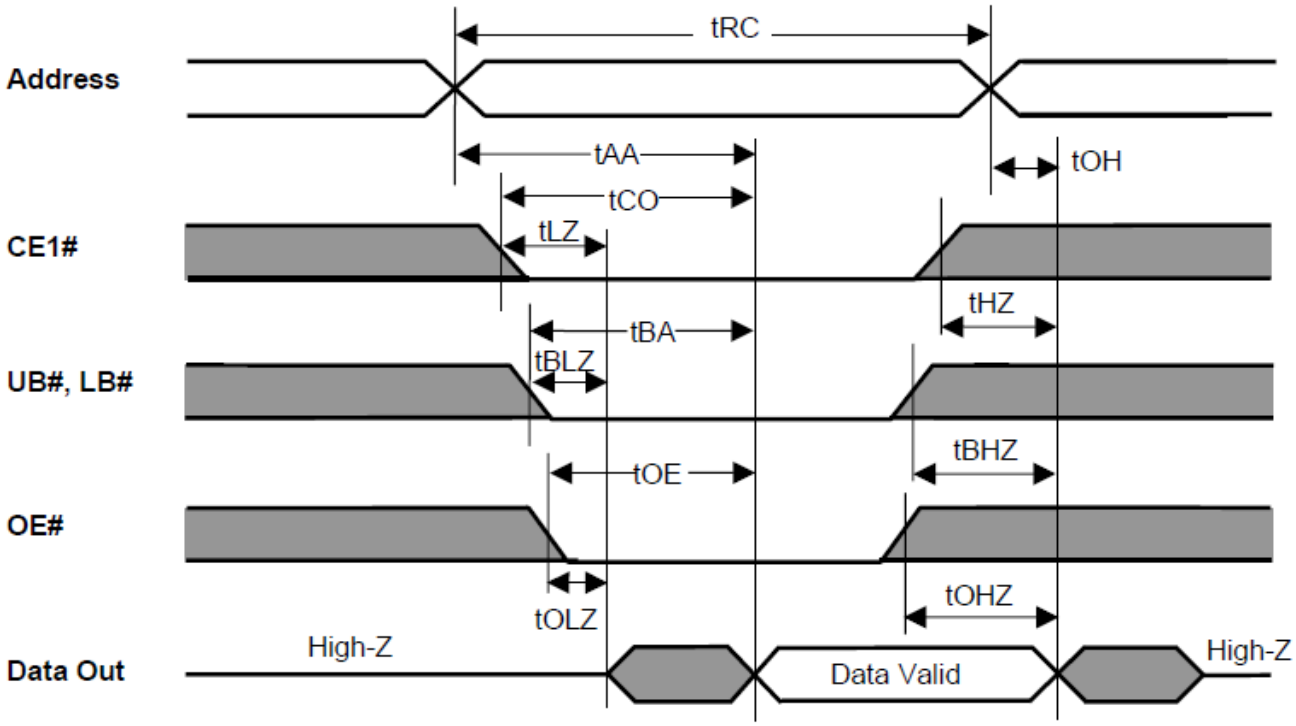
Parameter Name	Name	70		Unit
		Min	Max	
Read Cycle Time	t_{RC}	70	15k	ns
Address Access Time	t_{AA}	-	70	ns
Chip Enable Access Time (/CE1)	t_{CO1}	-	70	ns
Chip Enable Access Time (CE2)	t_{CO2}	-	70	ns
Output Enable access time	t_{OE}	-	45	ns
Data Byte Control Access Time	t_{BA}	-	70	ns
Chip Enable Low to Output in Low-Z	t_{LZ}	10	-	ns
Output enable Low to Output in Low-Z	t_{OLZ}	5	-	ns
Data Byte Control Low to Output in Low-Z	t_{BLZ}	10	-	ns
Chip Enable High to Output in High-Z	t_{HZ}	-	25	ns
Output Enable High to Output in High-Z	t_{OHZ}	-	25	ns
Data Byte Control High to Output in High-Z	t_{BHZ}	-	25	ns

Output Data Hold Time	t_{OH}	10	-	ns
Normal to Page Read Cycle Time	t_{PM}	70	15K	ns
Page Cycle Time	t_{PC}	25	-	ns
Page Mode Address Access Time	t_{PA}	-	25	ns

Read Cycle 1:Addressed Controlled[1)]

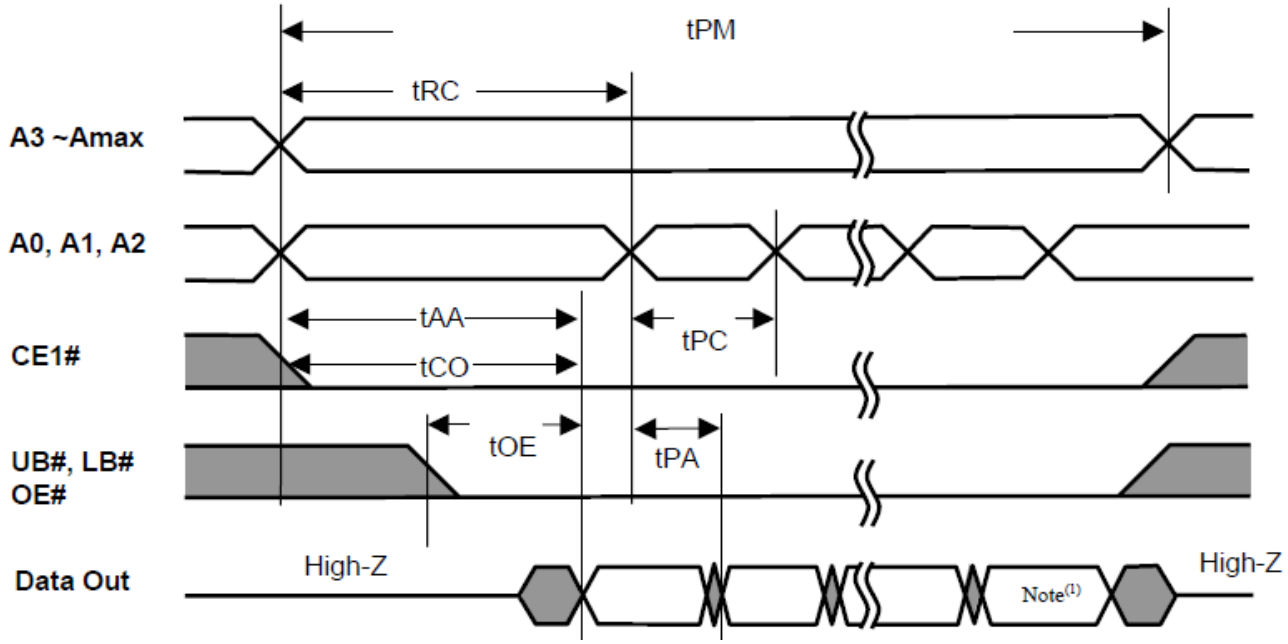


Read Cycle 2: /CE1 Controlled[2)]



Notes: ***1.*** *CE1# = OE# = VIL, CE2 = WE# = VIH, UB# or/and LB# = VIL* ***2.*** *CE2 = WE# = VIH*

Page Read Operation (CE2=/WE2=V_{IH}, 8 Words access)



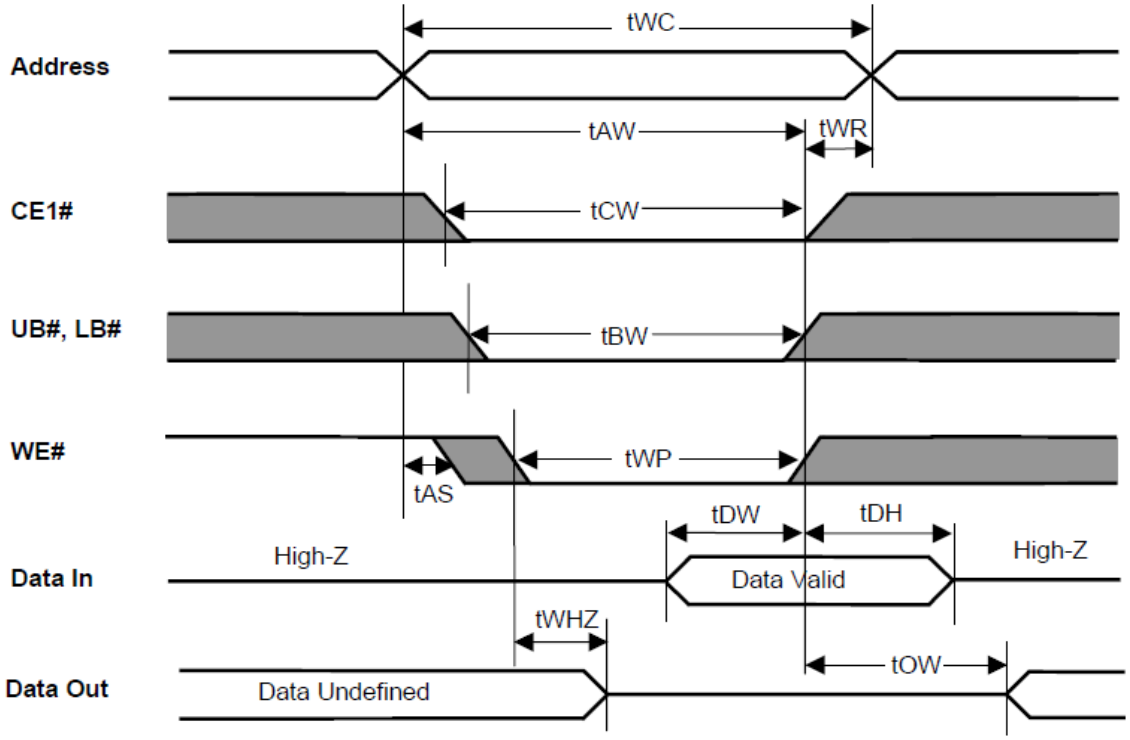
*Note **(1)** : Maxium 8 word. Random page read is supported within addresses(A0, A1,A2).*

***(2)** : CE2 and WE# are fixed high in Page Read Operation.*

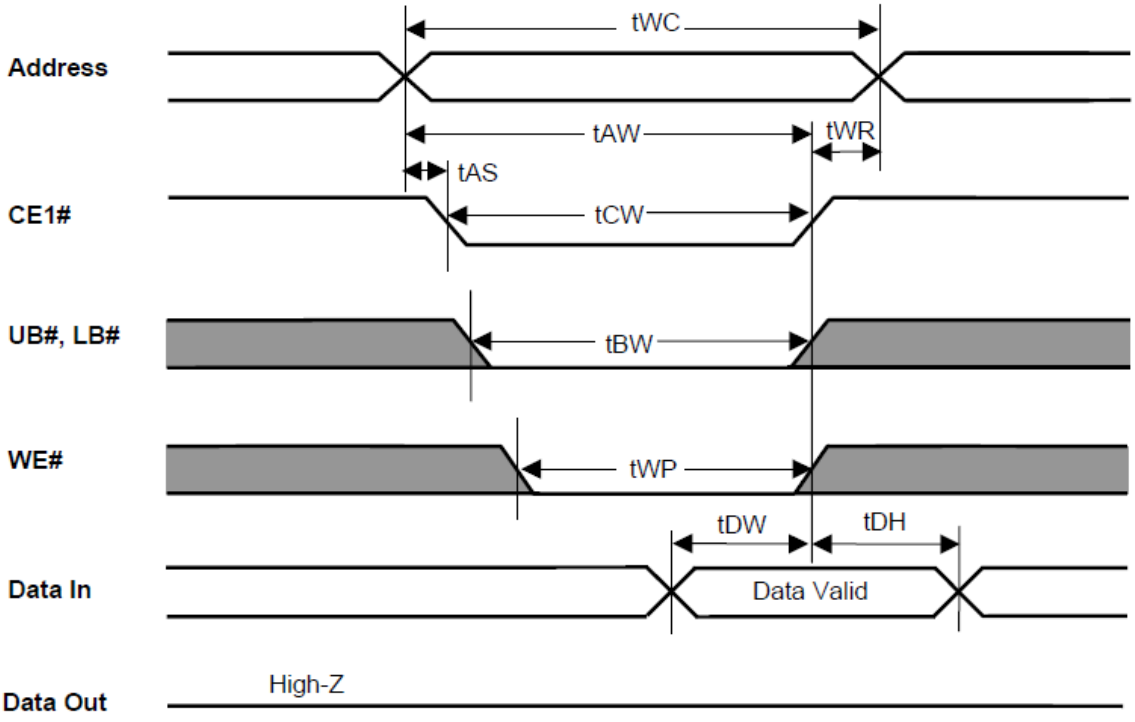
Write Cycle

Parameter Name	Name	70		Unit
		Min	Max	
Write Cycle Time	t_{WC}	70	-	ns
Write Pulse Width	t_{WP}	50	-	ns
Address Valid to End of Write	t_{AW}	60	-	ns
Chip Enable to End of Write	t_{CW}	60		ns
Data Byte Control to End of Write	t_{BW}	60	-	ns
Address Setup Ttime	t_{AS}	0	-	ns
Write Recovery Time	t_{WR}	0	-	ns
/WE Low to Output in High-Z	t_{WHZ}	-	20	ns
/WE High to Output in Low-Z	t_{OW}	5	-	ns
Data to Write Overlap	t_{DW}	30	-	ns
Data Hold Time	t_{DH}	0	-	ns

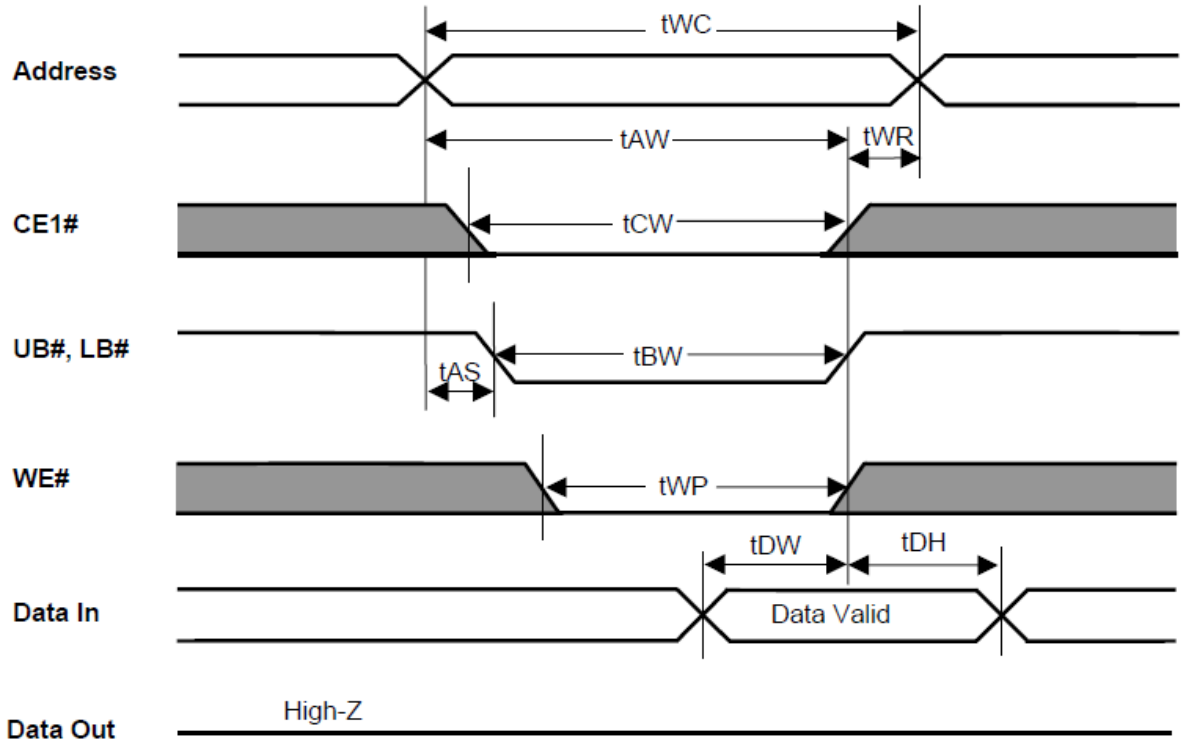
Write Cycle 1: /WE Controlled [1)2)]



Write Cycle 2: /CE1 Controlled [1)2)]

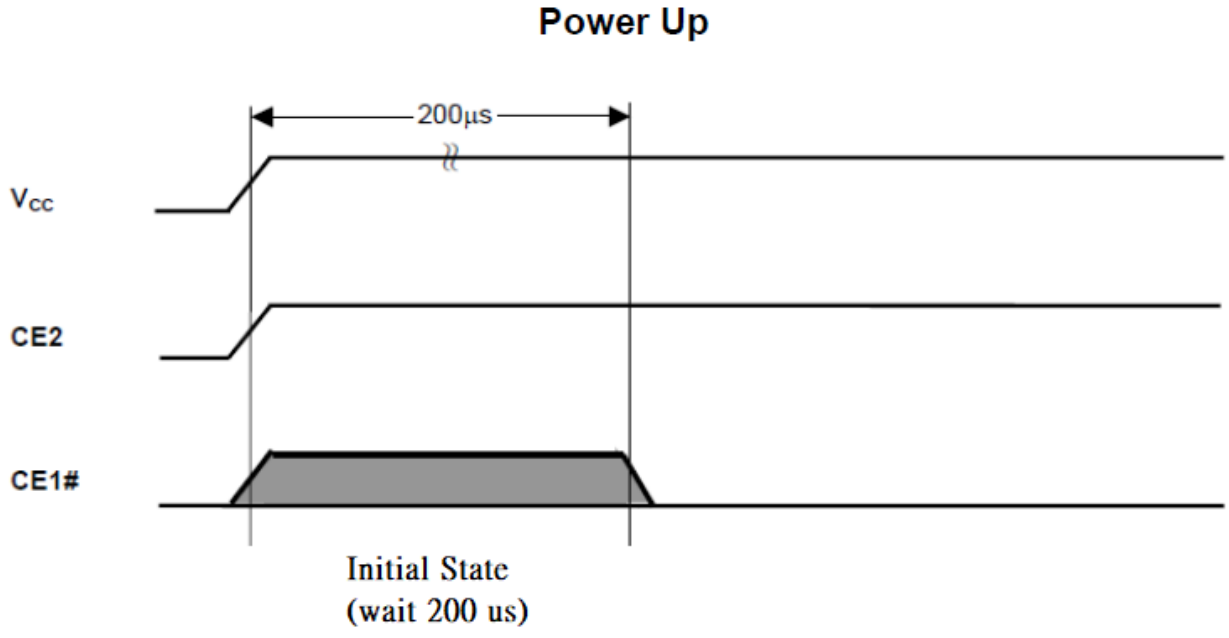


Write Cycle 3: /UB, /LB Controlled [1)2)]



*Notes: **1**. CE2 = VIH , **2**. CE2 = WE# = VIH*

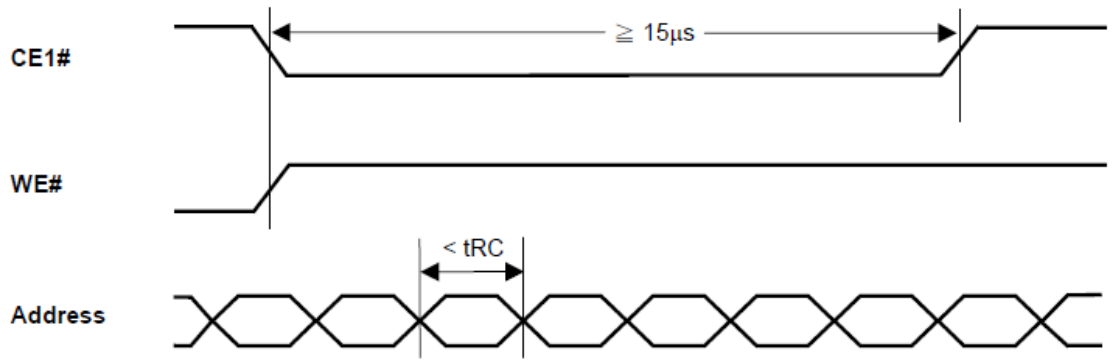
Power Up Mode



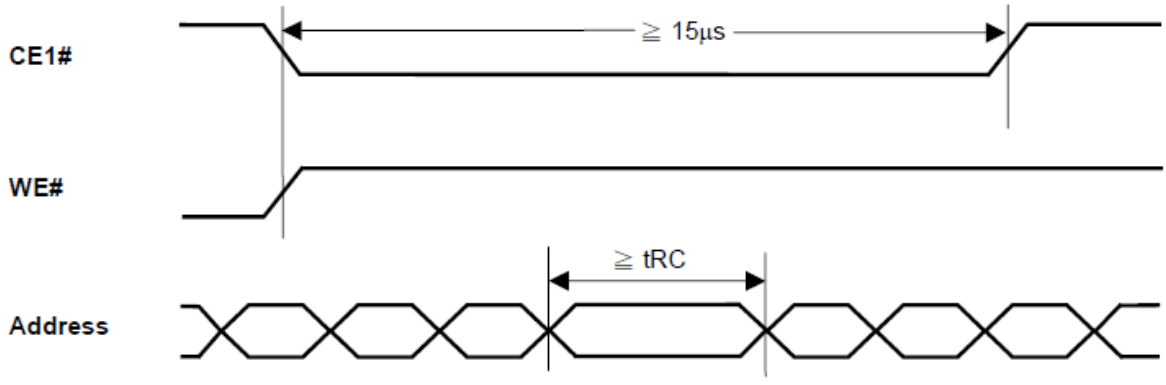
Avoid Timing

CS26LV16183 has a timing which is not supported at read operation. If your system has multiple invalid address signal shorter than t_{RC} during over 15μs at read operation shown as in Abnormal Timing, it requires a normal read timing at leat during 15 μs shown as in Avoidable timing 1 or toggle CE1# to high ($\geqq t_{RC}$) one time at least shown as in Avoidable Timing 2.

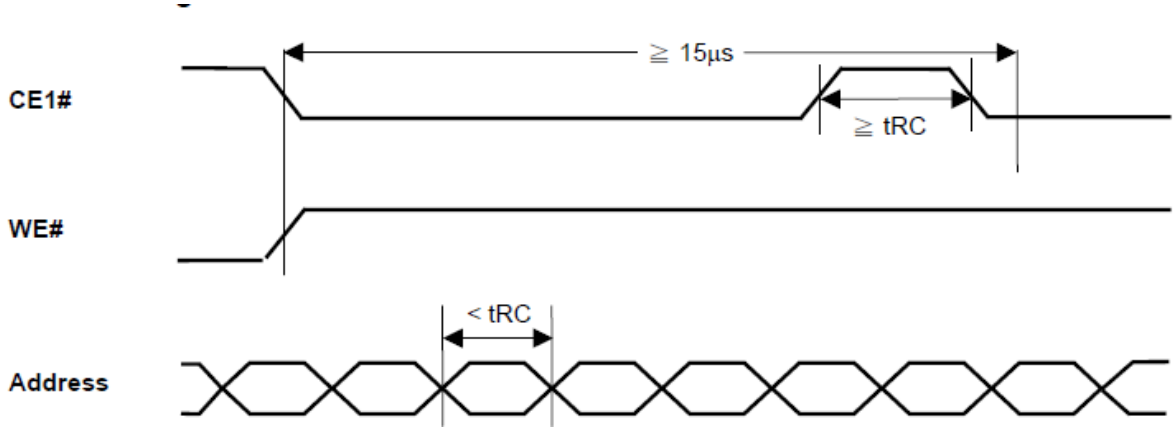
Abnormal Timing



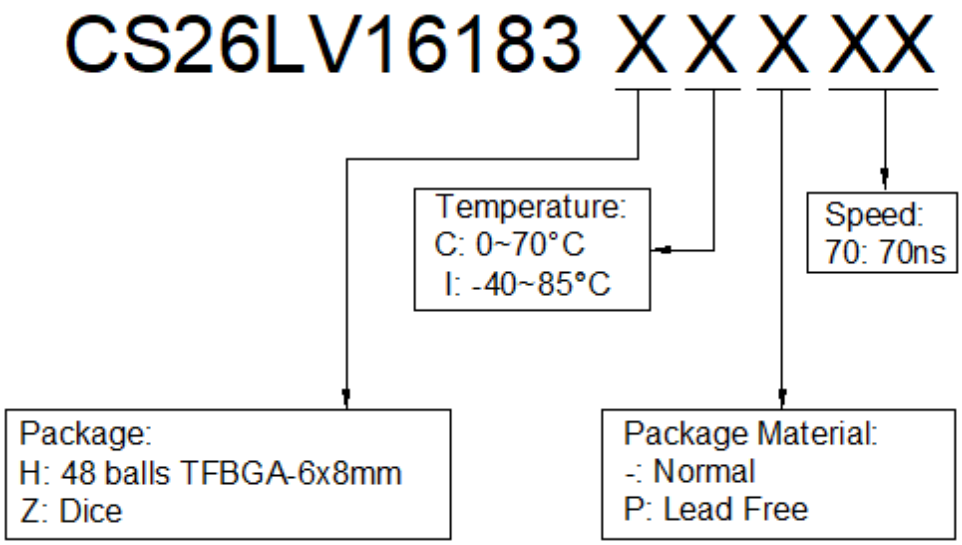
Avoidable Timing 1



Avoidable Timing 2

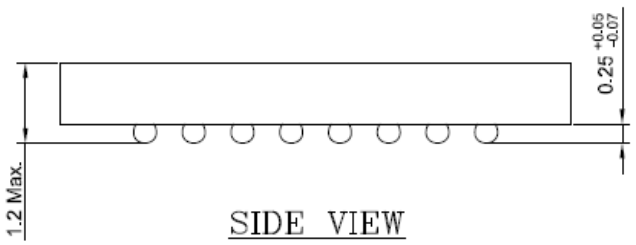


Order Information



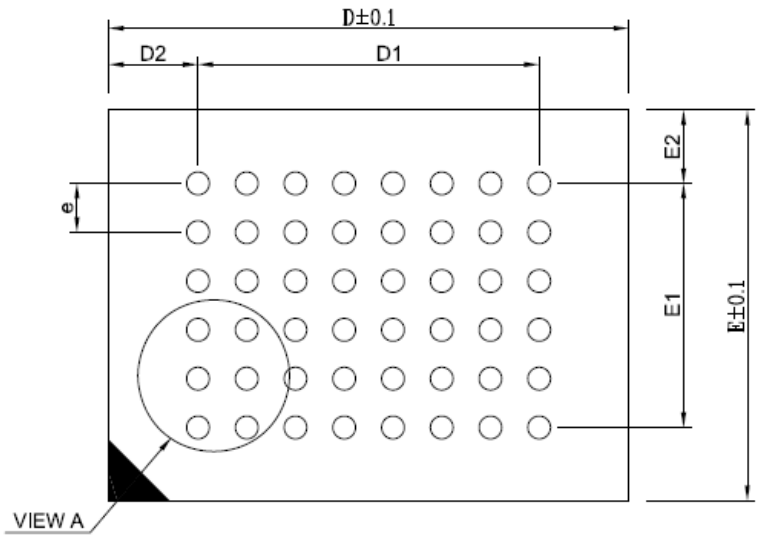
Package Outline

48 ball TFBGA-6x8mm

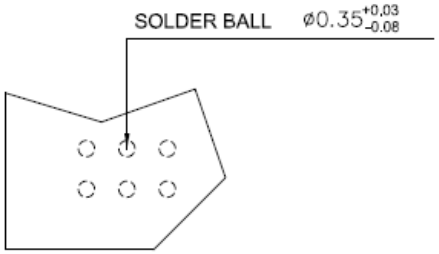


SIDE VIEW

BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125



TOP VIEW



VIEW A

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
   LINEAR : X.X = ±0.1
   X.XX = ± 0.05
   X.XXX = ± 0.025