Cover Sheet and Revision Status				
版別 (Rev.)	DCC No	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20170009	Jun 08, 2017	New issue	Hank Lin
2.0	20200019	Dec. 29, 2020	Revise ICC (operating current) 45ns- 20mA, 55ns- 20mA, 70ns- 15mA	Hank Lin

GENERAL DESCRIPTION

The CS16LV11245 is a high performance; high speed and super low power CMOS Static Random Access Memory organized as 65,536 words by 16bits and operates from a wide range of 4.5 to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed, super low power features and maximum access time of 55/70ns in 5.0V operation. Easy memory expansion is provided by an active LOW chip enable input (/CE) and active LOW output enable (/OE).

The CS16LV11245 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS16LV11245 is available in JEDEC standard 44-pin TSOP 2-400mil, 48-ball TFBGA 6*8mm.

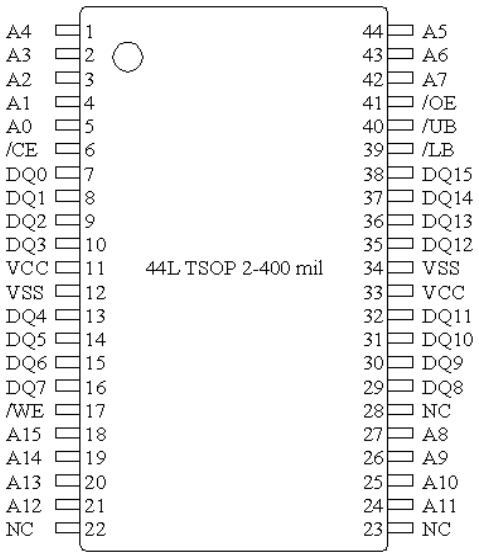
FEATURES

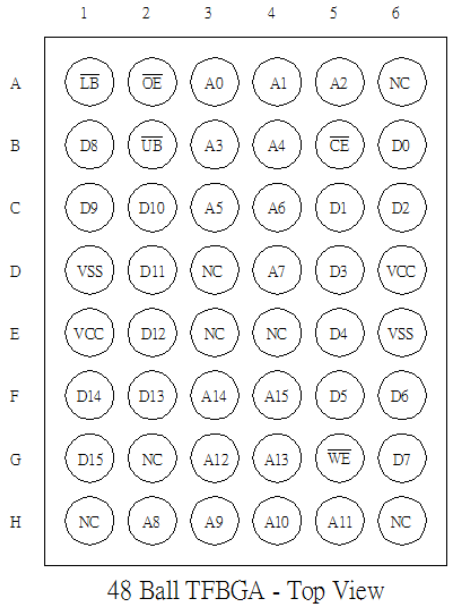
- Wide operation voltage : 4.5 ~ 5.5V
- Ultra-low power consumption :
  - operating current: 20mA (Max.) @t_{AA}=45ns
  - standby current : 2uA (Typ.)
- High speed access time: 45/55/70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supply voltage as low as 1.5V.

Product Family

Product Family	Operating Temp	V_{CC}. Range	Speed (ns)	Standby (Max)	Package Type
CS16LV11245	0~70ºC	4.5~5.5	45/55/70	8 uA (V_{CC} = 5.5V)	44L TSOP 2-400mil 48ball TFBGA 6*8mm
	-40~85ºC				

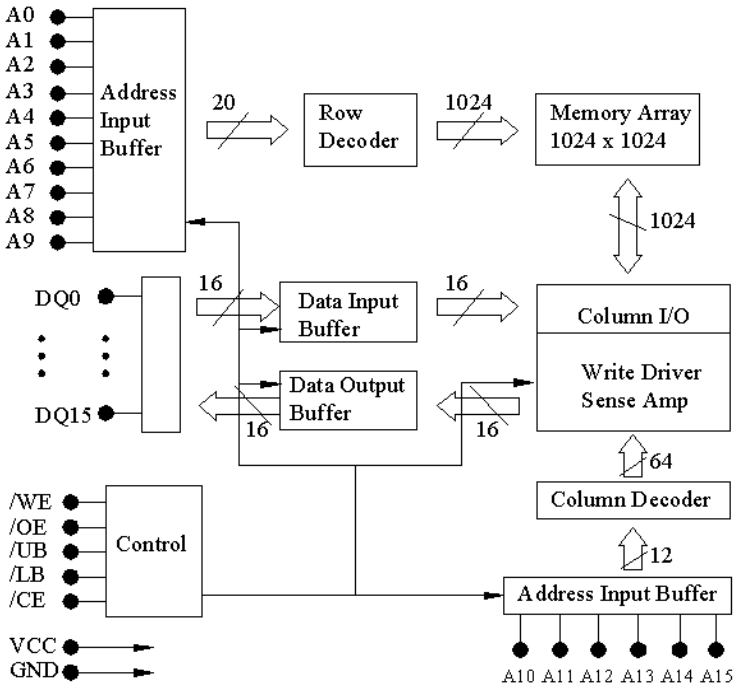
PIN CONFIGURATIONS





48 Ball TFBGA - Top View

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Type	Function
A0 – A15	Input	Address inputs for selecting one of the 65,536 x 16 bit words in the RAM
/CE	Input	/CE is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and in a standby power mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
/LB and /UB	Input	Lower byte and upper byte data input/output control pins.
DQ0~DQ15	I/O	These 16 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power	Power Supply
Gnd	Power	Ground

TRUTH TABLE

MODE	/CE	/WE	/OE	/LB	/UB	DQ0~7	DQ8~15	V_{CC} Current
Standby	X	X	X	H	H	High Z	High Z	I_{CCSB}, I_{CCSB1}
	H	X	X	X	X			
Output Disabled	L	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	L	L	L	D_{OUT}	D_{OUT}	I_{CC}
				H	L	High Z	D_{OUT}	I_{CC}
				L	H	D_{OUT}	High Z	I_{CC}
Write	L	L	X	L	L	D_{IN}	D_{IN}	I_{CC}
				H	L	X	D_{IN}	I_{CC}
				L	H	D_{IN}	X	I_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TBIAS	Temperature under Bias	-40 to +125	OC
TSTG	Storage Temperature	-60 to +150	OC
PT	Power Dissipation	1.0	W

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70°C	4.5V ~5.5V
Industrial	-40~85°C	4.5V ~ 5.5V

CAPACITANCE (1) (T_A = 25oC, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{DQ}	Input/output Capacitance	$V_{I/O}$=0V	8	pF

This parameter is guaranteed, and not 100% tested.

DC ELECTRICAL CHARACTERISTICS (T_A = 0℃ ~70℃, V_{CC} = 5.0V)

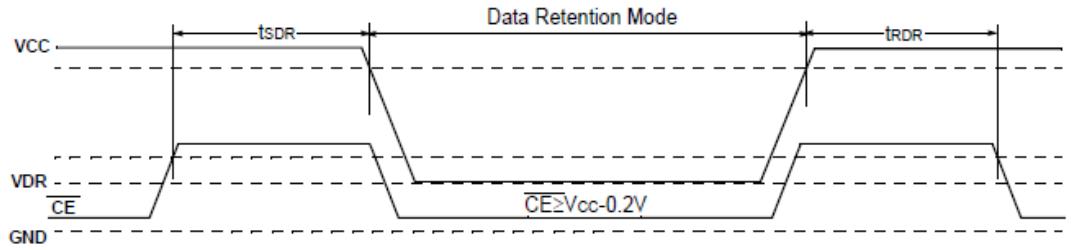
Name	Parameter	Test Condition		MIN	TYP (1)	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage (3)	V_{CC}=3.0V		-0.3		0.8	V
V_{IH}	Guaranteed Input High Voltage (2)	V_{CC}=3.0V		2.2		Vcc+ 0.5	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}		-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE=V_{Ih}, or /OE=$V_{Ih,\ or}$ /WE= V_{IL} V_{IO}=0V to V_{CC}		-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} =2.1mA				0.4	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -1.0mA		2.4			V
I_{CC}	Operating Power Supply Current	/CE=V_{IL}, I_{DQ}=0mA, F=F_{MAX} =1/ t_{RC}	45ns			20	mA
			55ns			20	
			70ns			15	
I_{CCSB}	TTL Standby Supply	/CE=V_{IH}, I_{DQ}=0mA,				0.3	mA
I_{CCSB1}	CMOS Standby Current	/CE≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V,			2	8	uA

1. *Typical characteristics are measured at Vcc=5V, T_A=25℃ and not 100% tested*
2. *Overshoot : VCC +2.0V in case of pulse width ≦20ns.*
3. *Undershoot : - 2.0V in case of pulse width ≦20ns.*
4. *Overshoot and undershoot are sampled, not 100% tested.*

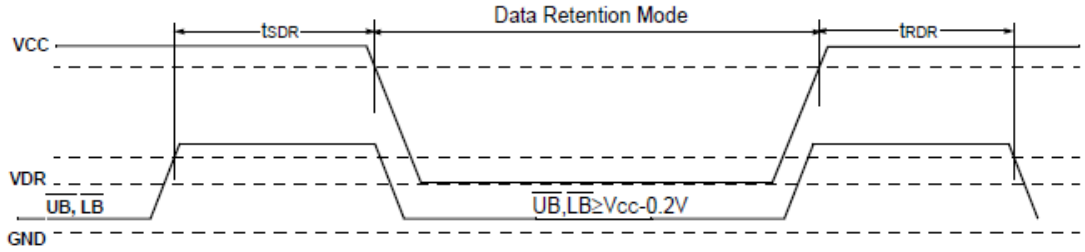
DATA RETENTION CHARACTERISTICS (T_A = 0℃ ~70℃)

Name	Parameter	Test Condition	MIN	TYP	MAX	Unit
V_{DR}	V_{CC} for Data Retention	/CE≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	1.5			V
I_{CCDR}	Data Retention Current	/CE≧V_{CC}-0.2V, V_{CC} =1.5V V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V		2	6	uA
T_{CDR}	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC}			ns

LOW V_{CC} DATA RETENTION WAVEFORM (1) (/CE Controlled)



LOW V_{CC} DATA RETENTION WAVEFORM (2) (/UB, /LB Controlled)



AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Level	0.5Vcc
Output Load	See FIGURE 1A and 1B

KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

AC TEST LOADS AND WAVEFORMS

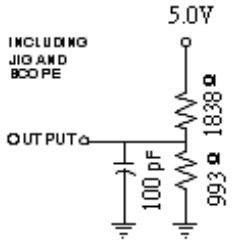


FIGURE 1A

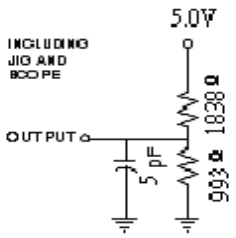


FIGURE 1B

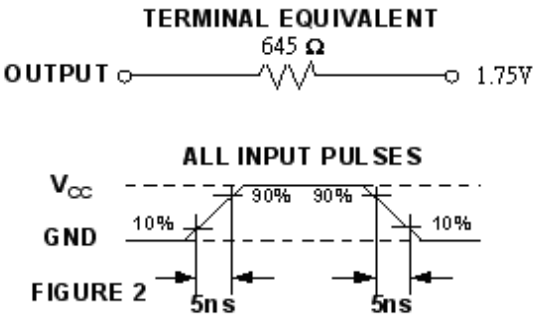


FIGURE 2

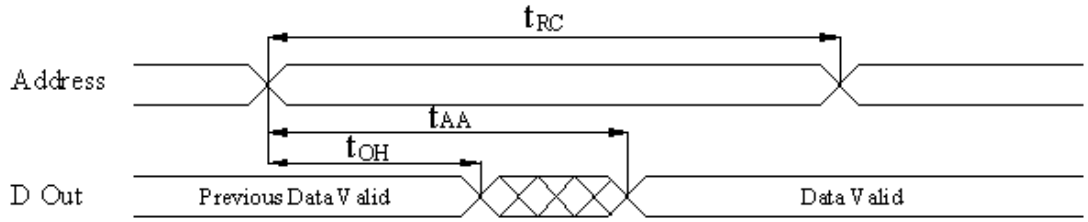
AC ELECTRICAL CHARACTERISTICS (T_A = 0℃ ~70℃ ; V_{CC}=5.0V)

READ CYCLE

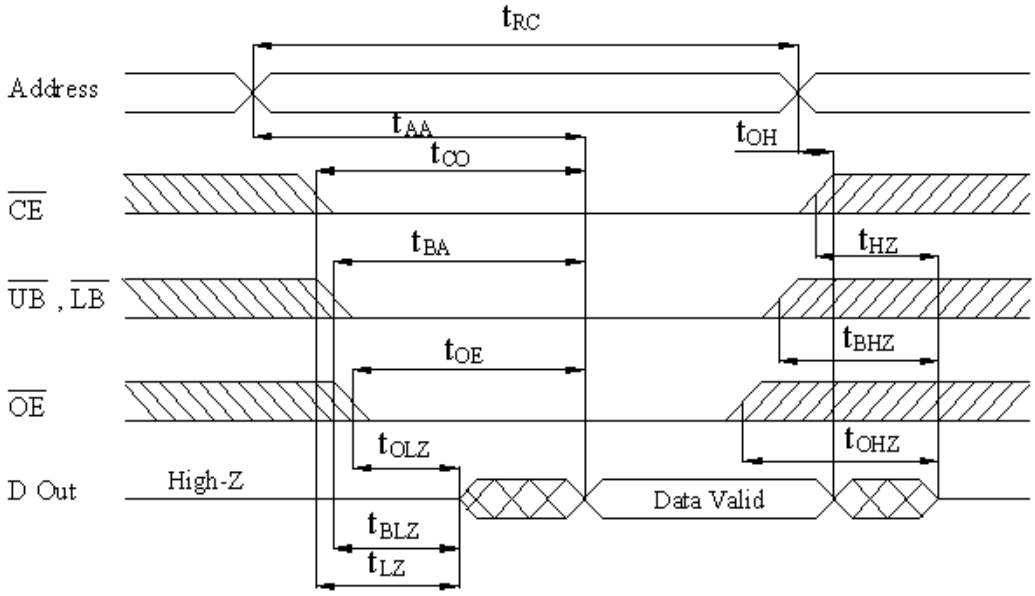
Parameter Name	Description	-45		-55		-70		Unit
		MIN.	MAX	MIN.	MAX	MIN.	MAX	
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address Access Time		45		55		70	ns
t_{ACS}	Chip Select Access Time (/CE)		45		55		70	ns
t_{BA}	Data Byte Control Access Time (/LB, /UB)		45		55		70	ns
t_{OE}	Output Enable to Output Valid		22		25		35	ns
t_{CLZ}	Chip Select to Output Low Z (/CE)	10		10		10		ns
t_{BE}	Data Byte Control to Output Low Z (/LB, /UB)	5		5		5		ns
t_{OLZ}	Output Enable to Output in Low Z	5		5		5		ns
t_{CHZ}	Chip Deselect to Output in High Z (/CE)	0	18	0	20	0	25	ns
t_{BDO}	Data Byte Control to Output High Z (/LB, /UB)		18	0	20	0	25	ns
t_{OHZ}	Output Disable to Output in High Z		18	0	20	0	25	ns
t_{OH}	Out Disable to Address Change	10		10		10		ns

SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE1



READ CYCLE2



NOTES:

1. *t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
2. *At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.*

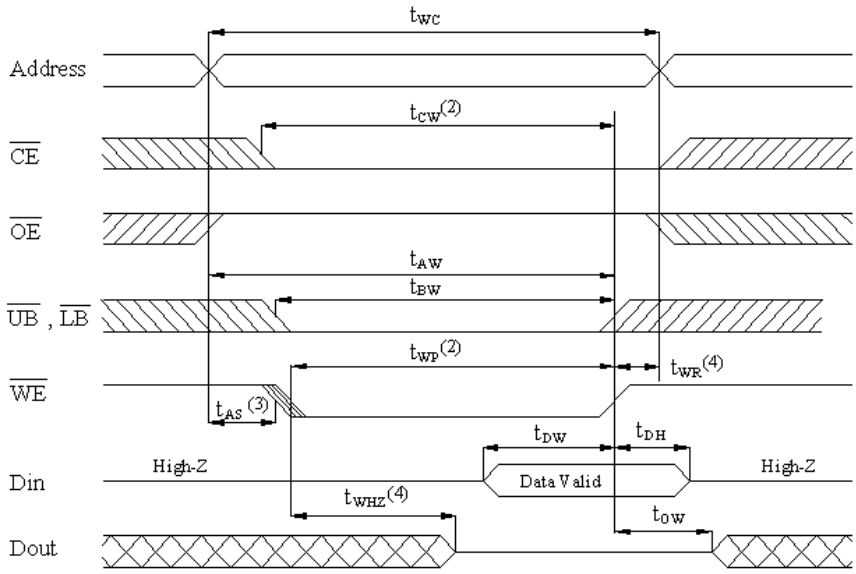
AC ELECTRICAL CHARACTERISTICS (T_A = 0℃ ~70℃；V_{CC}=5.0V)

WRITE CYCLE

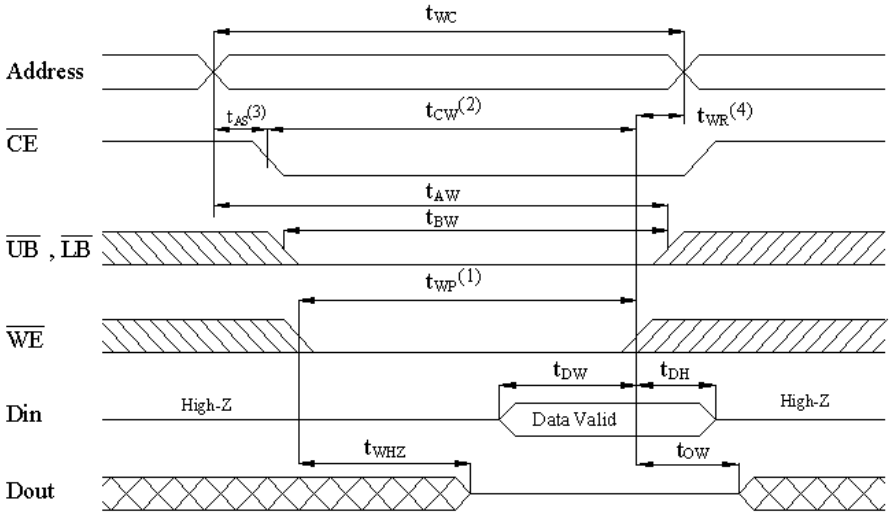
JEDEC Parameter Name	Parameter Name	Description	-45		-55		-70		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	45	-	55	-	70	-	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	35	-	45	-	60	-	ns
t_{AVWL}	t_{AS}	Address Setup Time	0	-	0	-	0	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	35	-	45	-	60	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	35	-	40	-	55	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time (/CE, /WE)	0	-	0	-	0	-	ns
t_{BW}	t_{BW}	Data Byte Control to End of Write (/LB, /UB)	35	-	45	-	60	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	-	18	-	20	-	25	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25	-	25	-	30	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5	-	5	-	5	-	ns

SWITCHING WAVEFORMS (WRITE CYCLE)

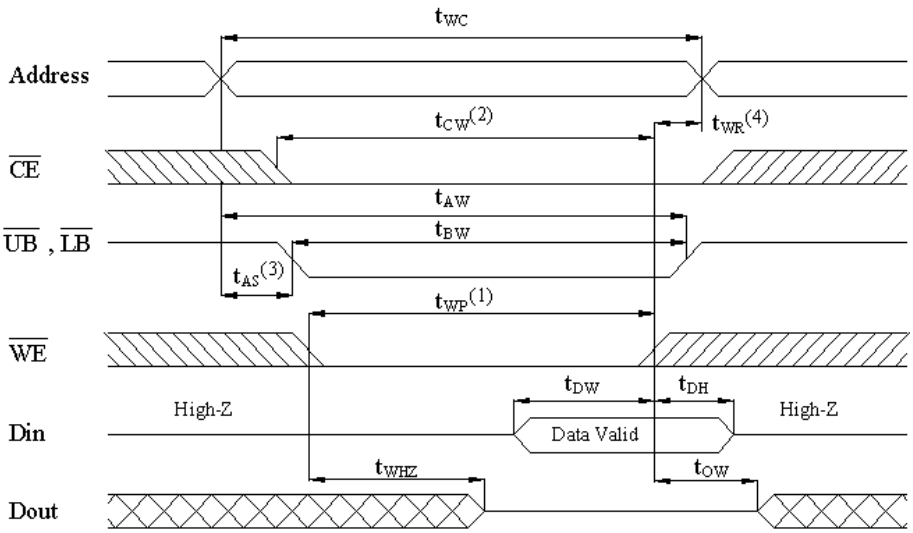
WRITE CYCLE1 (/WE CONTROLLED)



WRITE CYCLE2 (/CE CONTROLLED)



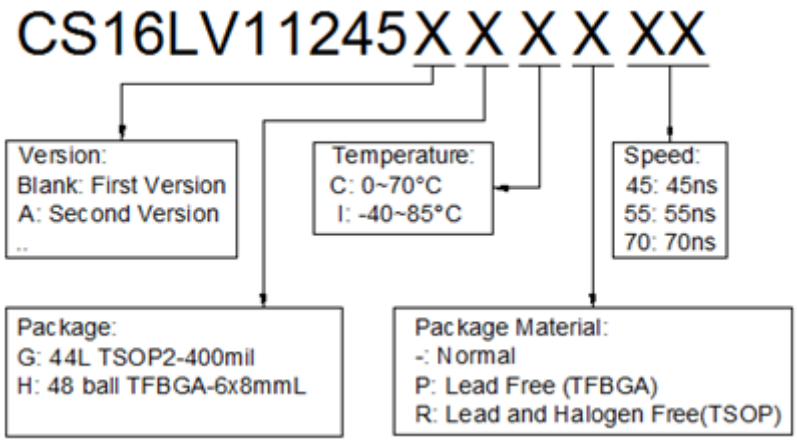
WRITE CYCLE3 (/UB, /LB CONTROLLED)



NOTES:

1. *A write occurs during the overlap (t_{WP}) of low /CE and low /WE. A write begins when /CE goes low and /WE goes low with asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CE goes high and /WE goes high. The tWP is measured from the beginning of the write to the end of write.*
2. *t_{CW} is measured from the /CE going low to end of write.*
3. *t_{AS} is measured from the address valid to the beginning of write.*
4. *t_{WR} is measured from the end or write to the address change. TWR applied in case a write ends as /CE or /WE going high.*

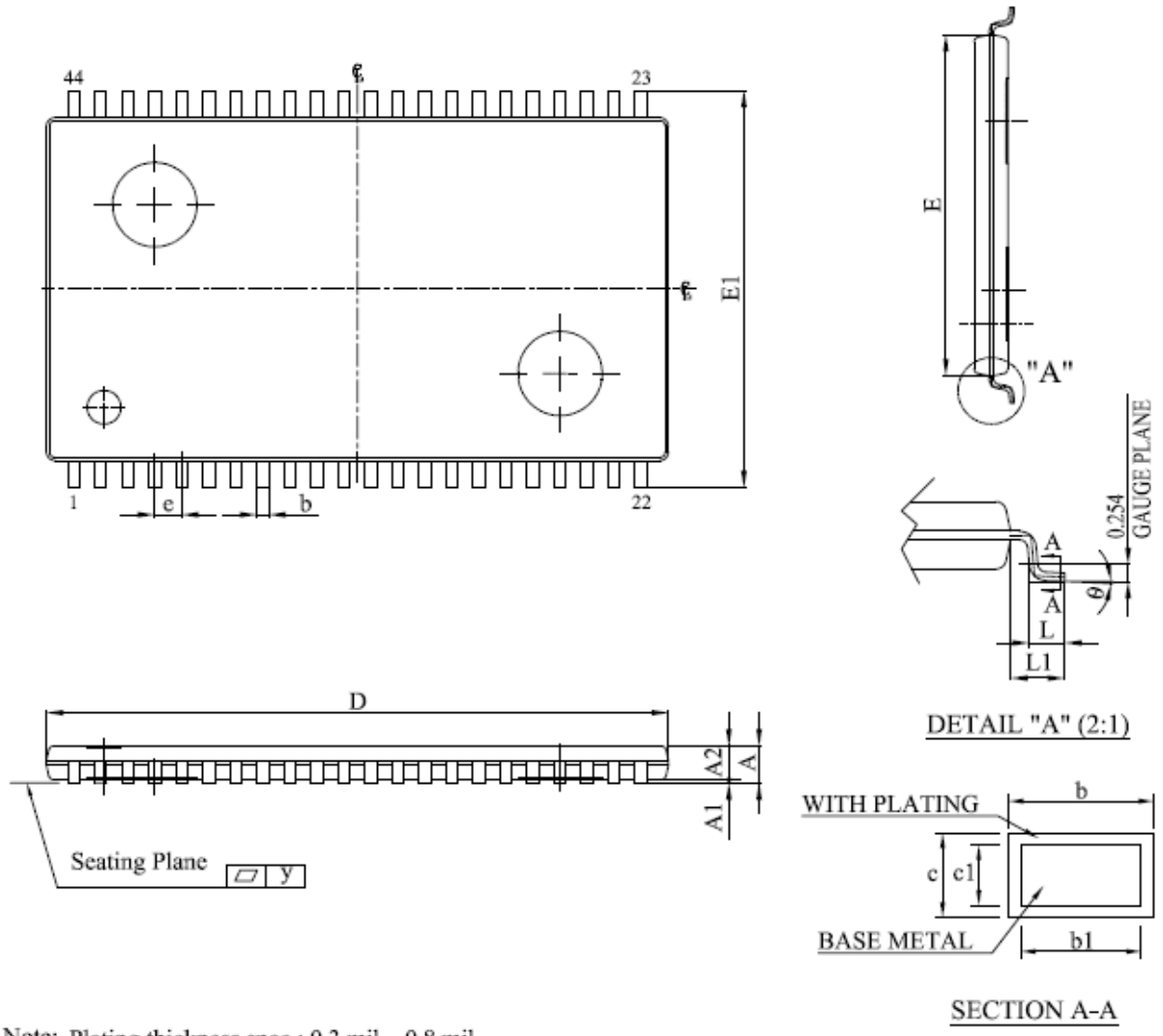
ORDER INFORMATION



Note: Package material code "R" meets ROHS

PACKAGE OUTLINE

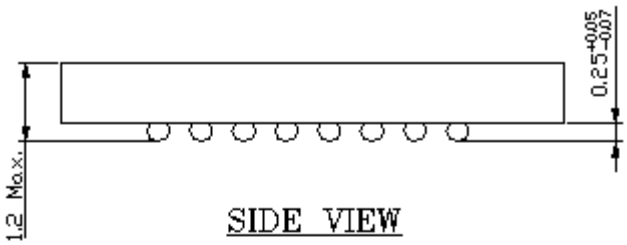
44L TSOP2-400mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

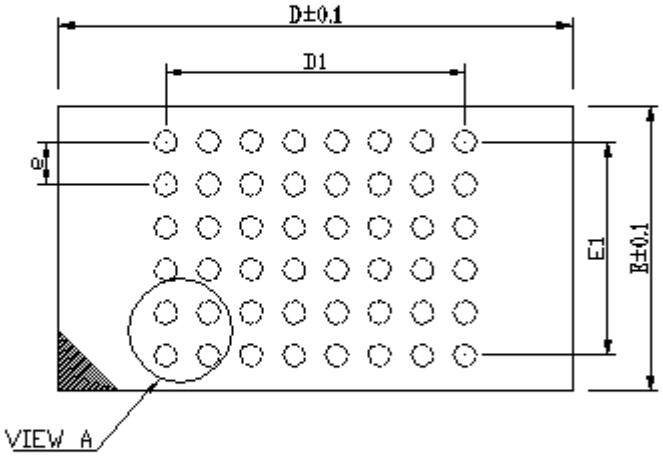
SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	Θ
mm	Min.	1.00	0.05	0.95	0.30	0.30	0.12	0.12	18.31	10.06	11.56	0.70	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	–	–	–	–	18.41	10.16	11.76	0.80	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.45	0.40	0.21	0.16	18.51	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.012	0.012	0.005	0.005	0.721	0.396	0.455	0.0275	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	–	–	–	–	0.725	0.400	0.463	0.0315	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.018	0.016	0.008	0.006	0.729	0.404	0.471	0.0355	0.0237	0.0355	0.004	8°

48 ball TFBGA-6x8mm

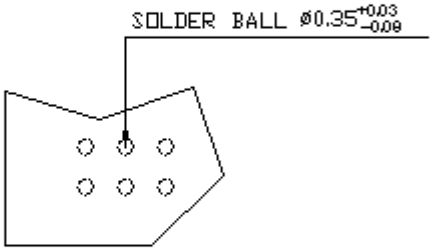


SIDE VIEW

BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75



TOP VIEW



VIEW A

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL 'N' IS THE NUMBER OF SOLDER BALLS.